MAINTENANCE MANUAL

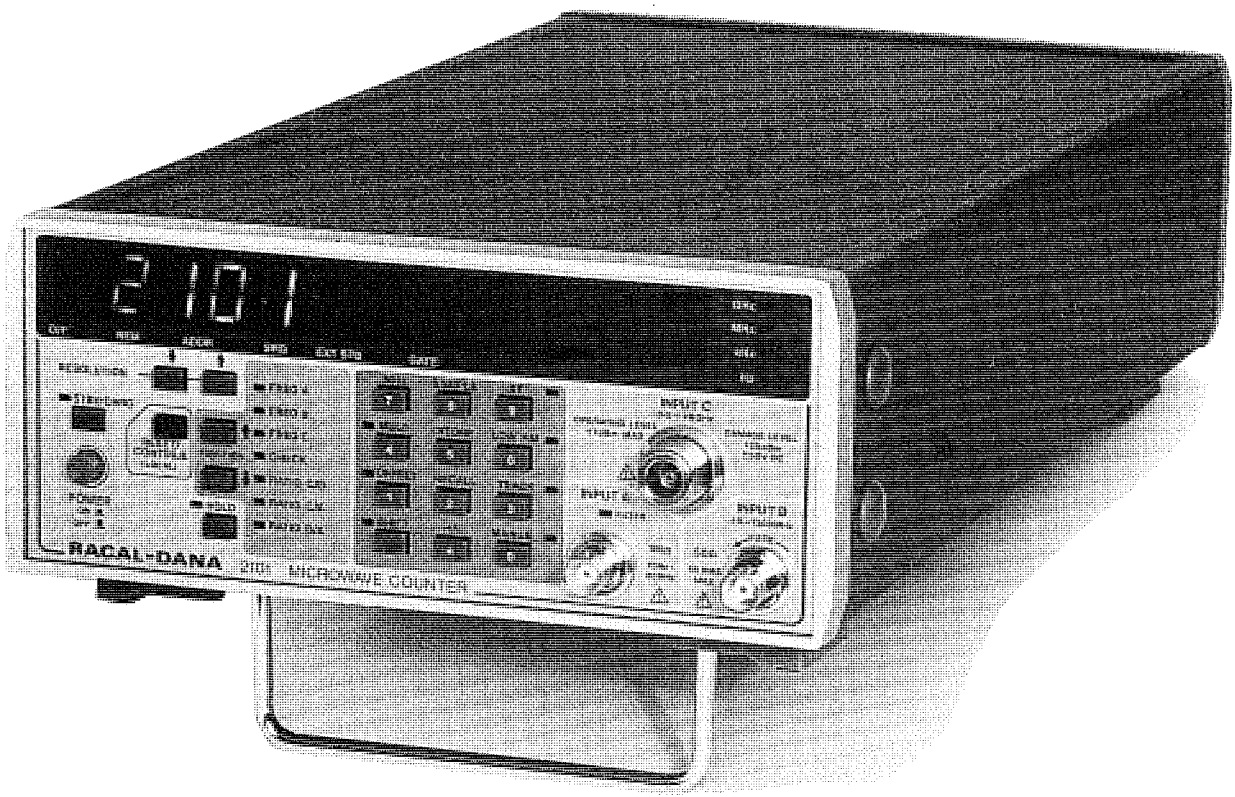
2101

20 GHz
MICROWAVE COUNTER

RACAL INSTRUMENTS LTD

RACAL

The Electronics Group



RACAL

A2037

Microwave Counter: 2101

HANDBOOK AMENDMENTS

Amendments to this handbook (if any), which are on coloured paper for ease of identification, will be found at the rear of the book. The action called for by the amendments should be carried out by hand as soon as possible.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

SECTION 8 PARTS LIST AND CIRCUIT DIAGRAMS

LIST OF TABLES

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

SECTION 1 TECHNICAL SPECIFICATION

Technical Specifications

Input A

Frequency Range	10Hz to 100MHz
Sensitivity (rms)	20mV (to 80MHz) 30mV (at 100MHz)
Input Impedance	1MΩ/35pF
Maximum Input	260V (DC + AC rms) to 2kHz, decreasing to 10V rms at 50kHz and above
Filter	Low pass filter (50kHz)

Input B

Frequency Range	40MHz to 1.3GHz
Sensitivity	10mV (to 1GHz) 50mV (at 1.3GHz)
Input Impedance	50Ω nominal
Operating Range	10mV to 5V rms
Damage Overload	7V rms (protected by fuse)
VSWR	<2.3 : 1 (1GHz)

Input C (Microwave Channel)

Frequency Range	500MHz to 20GHz
Sensitivity	-32dBm (to 12.4GHz) -27dBm (at 20GHz)
Operating Level	+7dBm
Damage Level	+25dBM peak (+33dBm with Option 11)
Input Connector	Precision type N female
VSWR	<2:1 (to 10GHz) <3:1 (to 20GHz)
AM Tolerance	Any modulation depth

FM Tolerance

Mode	Modulation Rate	FM Tolerance Max. Deviation
Automatic		
Normal	1kHz to 10MHz	20MHz pk-pk
Low FM	45Hz to 10MHz	20MHz pk-pk
Track	300kHz to 10MHz	20MHz pk-pk
Manual	1kHz to 10MHz	60MHz pk-pk*

* If set within ±1MHz

Acquisition Time

Mode	Acquisition Time
Automatic	
Normal	<125mSec
Low FM	<1.25mSec
Track	<60mSec
Manual	<20mSec

Tracking Speed

Mode	Tracking Speed
Normal	1MHz/Sec
Low FM	80kHz/Sec
Track	1GHz/Sec

Spillback	Typically -55dBm (-70dBm in quiet mode)
Amplitude Discrimination (Typical)	6dB for signals within 500MHz 20dB for signals at any frequency

IF Output

Available when measurements are made using Input C in Manual Mode. Available intermittently during gate time in Auto Mode.

Frequency Range	41MHz to 112MHz
Output Level	-10dBm nominal
Output Impedance	50Ω nominal
Reverse Damage Level	400V pk to 500Hz, decreasing to 10V rms at 30kHz and above

Measurement Modes

Frequency A and B

Range Frequency A	10Hz to 100 MHz
Range Frequency B	40MHz to 1.3GHz
Digits Displayed	3 to 10 digits
LSD Displayed (Hz)	$Fx10^{-D}$ (F=frequency rounded up to next decade, D=no. of digits)
Resolution (Hz)	$\pm LSD^{+} \pm \left[\frac{1.4 \times \text{Trig Error}^{*}}{\text{Gate Time}}\right] \times \text{Ratio}$
Accuracy (Hz)	± Resolution ± (Timebase Error x Freq)

Frequency C

Range	500MHz to 20GHz
LSD Display (Resolution)	0.1Hz to 1MHz (selectable)
Accuracy	± Resolution ± Timebase error x Frequency ± Residual stability*

Ratio B/A, C/A/, C/B

Software Ratios. (Hardware ratio also available for B/A using SF91)

Range (B/A)	$\frac{\text{40MHz to 1.3GHz}}{\text{10Hz to 80MHz}}$
Range (C/A)	$\frac{\text{500MHz to 20GHz}}{\text{10Hz to 80MHz}}$
Range (C/B)	$\frac{\text{500MHz to 20GHz}}{\text{40MHz to 1.3GHz}}$
LSD Displayed	$R \times 10^{-D}$ (R=Ratio rounded up to next decade, D=number of digits)
Resolution (ppm)	Sum of the 2 resolutions expressed in ppm
Accuracy (ppm)	Sum of the 2 accuracies expressed in ppm
Check	10MHz frequency standard displayed

Features

Manual	For fastest measurement and data output rates, Manual Mode suspends automatic operation and microprocessor calculates optimum internal local oscillator frequency and harmonic number from a user-entered centre frequency
	NB user enters centre frequency to within ±20MHz of input frequency (±3MHz below 1GHz)
Low FM	For accepting very low modulation rates
Track	Track mode selects the fastest possible acquisition cycle and tracks the movement of fast moving input frequencies

Maths

Multiply	Displays the measured frequency multiplied by an entered number
Offset	Allows a stored or keyboard entered frequency to be added or subtracted from the measured signal
Smooth	Displays the optimum resolution relevant to the stability of the input signal

GPIB

GPIB Interface	Designed to comply with IEEE-STD-488.1(1987) and IEEE-STD-488.2(1987)
Control Capability	All functions/controls programmable except power on/ off and standby/charge
Output	Engineering format having 12 digits and exponent
Read Rate	5 to 18 per Sec. dependant on measurement function. Faster dump mode available
IEEE-STD-488 Subsets	SH1, AH1, T5, TE0, L4, LE0, SR1. RL1, PPO, DC1, DT1, CO, E2

+ n=1 for 3-5 and 10 digits or 2 for 6-9 digits

* See definitions

Timebase Specifications

Internal Timebase (PX0)

Frequency	10MHz
Aging Rate	2 x 10^{-6} in the first year
Temp. Stability	1x10^{-5} over 0-50°C range

Frequency Standard Output

Frequency	10MHz
Amplitude	TTL levels giving approximately 1V pk-pk into 50Ω

External Standard Input

Frequency	10MHz (see also Option 10)
Signal Range	100mV rms to 10V rms
Damage Level	10V rms
Input Impedance	1kΩ nominal for signals <1V pk-pk
	500Ω nominal for signals ≥10V pk-pk
Coupling	AC coupled

General Specifications

Single Cycle (Hold)	Enables a single measurement to be initiated and held
Gate Times	Automatically determined depending on resolution selected
Range	1mSec to 20Sec (10 Sec maximum for channel C)
Sample Rate	Selectable display and data output rates
Display	13 digit high brightness 14mm LED display. Separate indicators for GHz, MHz, kHz and Hz

Power Requirements

Voltage	90 to 127V, 193 to 253V (externally selectable)
Frequency	45 to 440Hz
Power Rating	40VA max
Operating Temp. Range	0 to 50°C 0 to 40°C (with batteries)
Storage Temp. Range	-40 to +70°C -40 to +60°C (with batteries)
EMC/RFI	Meets the requirements of MIL-STD-461 RE02 to 1.3GHz and CE03
Safety	Designed to meet the requirements of IEC348 and follow the guidelines of UL1244
Weight	Net 5.5kg excluding battery Net 8:4kg including battery
Normal Dimensions	See back page
Shipping Dimensions	260mm (H) x 355mm (W) x 610mm (D)

Options

Option 01 Rear Panel Inputs

Connections to input channels A, B and C an be made at rear.

Option 04T Temperature Compensated Crystal Oscillator

Frequency	10MHz
Aging Rate	3 x 10^{-7} per month 1 x 10^{-6} in the first year
Temp. Stability	1 x 10^{-6} over the range 0°C to +40°C (Operable to +50°C)

Option 04A Ovened Oscillator

Frequency	10MHz
Aging Rate	3×10^{-9} per day averaged over 10 days after 3 months continuous operation
Temp. Stability	$\pm 3 \times 10^{-9}$ per °C averaged over the range 0°C to +45°C (operable to +50°C)

Option 04B High Stability Ovened Oscillator

Frequency	10MHz
Aging Rate	5×10^{-10} per day averaged over 10 days after 3 months continuous operation
Temp. Stability	$\pm 6 \times 10^{-10}$ per °C averaged over range 0°C to +45°C (operable to +50°C)

Option 07 Rechargeable Battery Pack and External DC Operation

Battery Life	Up to 30 hours on battery save/ standby (typical 3 hours continuous at 25°C)
Battery Condition	Display indicates battery low
External DC	11 to 16V via socket on rear panel

Option 10 Reference Frequency Multiplier

Input Frequency	1,2,5 or 10MHz ($\pm 1 \times 10^{-5}$)

Option 11 Power Limiter

Fitted internally to increase Input C protection

Max. CW power	+36dBm to 18GHz decreasing to +33dBm at 20GHz
Sensitivity Loss	3 to 4dB depending on frequency

Note: further options/accessories listed on back page.

Definitions

Trigger Error rms

$$\text{Trigger Error} = \frac{[E_t^2 + E_n^2]^{1/2}}{\text{Slew rate at Trigger Point (V/Sec)}}$$

E_t = Input amplifier rms noise (typically 100µV rms in 100MHz bandwidth)

E_n = Input signal rms noise in 100MHz bandwith

Residual Stability (channel C only)

Residual stability (rms) = 1 LSD for resolutions 0.1Hz to 1kHz, negligible above 1kHz

Software Ratio Measurements

Counter measures denominator first according to the number of digits selected. It then measures the numerator with the same value of LSD, subject to the maximum resolution possible.

ORDERING INFORMATION

2101	20GHz Microwave Counter (includes GPIB)

OPTIONS AND ACCESSORIES

01*	Rear Panel Inputs	11-9010
04T**	TCXO	11-1713
04A**	Oven Oscillator	11-1710
04B**	High Stability Oven Oscillator	11-1711
07 §	Battery Pack (includes handles)	11-9009
10	Reference Frequency Multiplier	11-1645
11	Input Power Limiter	11-9011

60	Handles	11-1730
60A	Rack Mounting Kit (Fixed Single)	11-1648
60B***	Rack Mounting Kit (Fixed Double)	11-1649
61	Carrying Case	15-7001
61M	Protectomuff Case	15-7000
65	Chassis Slides (inc. Rack Mounts)	11-1716
68	Telescopic Antenna	23-9020
69	1.3GHz Fuse (Pkt 5)	11-1718
93	High Impedance 100MHz Probe	23-9104

§ The battery pack option replaces the GPIB normally fitted.

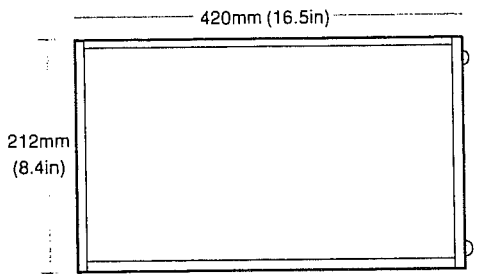
* Fitting Option 01 may affect certain input specifications and Option 11 now external.

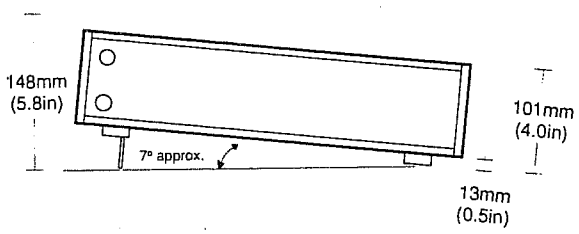
** Only one frequency standard may be fitted at any one time. The standard reference will be supplied unless Option 04T, 04A or 04B is specified.

*** For use with 1990 Series Counter. The 2101 must be at left side of rack.

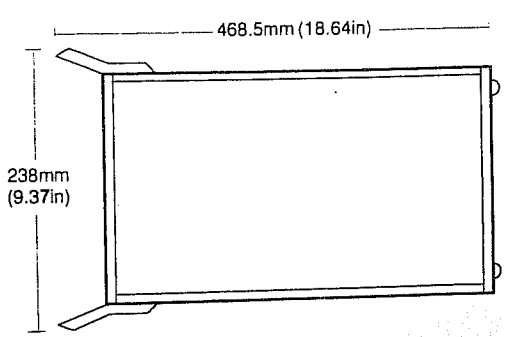
SUPPLIED ACCESSORIES

Power Cord
Spare Fuse
Operator's Manual
Spare 1.3GHz Fuse





With Optional Handles Fitted



SECTION 2 GENERAL DESCRIPTION

INTRODUCTION

1 The Racal-Dana microwave counter Model 2101 is a microprocessor-controlled instrument offering high-accuracy measurements with a comprehensive range of facilities. These facilities include Automatic/Manual Operation, Tracking, Offset, Multiply, and Store and Recall.

MEASUREMENT FUNCTIONS

Frequency A Function

2 The Frequency A Function is used to measure the frequency of the signal applied to INPUT A. A resolution of up to ten digits can be selected with a gate time of 1 millisecond to 20 seconds depending on the resolution selected.

Frequency B Function

3 The Frequency B Function is used to measure the frequency of the signal applied to INPUT B. A resolution of up to ten digits can be selected with a gate time of 1 millisecond to 20 seconds depending on the resolution selected.

Frequency C Function

4 The Frequency C Function is used to measure the frequency of the signal applied to INPUT C. A resolution of 0.1 Hz to 1 MHz can be selected with a gate time of 1 millisecond to 10 seconds depending on the resolution selected and frequency being sampled.

Ratio C/B Function

5 The Ratio C/B Function is used to measure the ratio of the frequency applied to INPUT C to that applied to INPUT B.

Ratio C/A Function

6 The Ratio C/A Function is used to measure the ratio of the frequency applied to INPUT C to that applied to INPUT A.

Ratio B/A Function

7 The Ratio B/A Function is used to measure the ratio of the frequency applied to INPUT B to that applied to INPUT A.

CHECK FUNCTION

8 The check function measures and displays the internal standard frequency to confirm counter operation. With the CHECK function selected a number of functional tests of the instrument's circuits can be made without the use of additional test equipment (Special Functions 71 to 75). Although these tests do not check the instrument's performance to its published specification, they can be used to verify that the instrument is operating correctly.

SIGNAL INPUT CHANNELS

9 Signal input channels A, B and C are fully independent.

The main characteristics of INPUT A are as follows:

(1) Frequency range of 10 Hz to 80 MHz.

(2) BNC input connector

(3) Input impedance of 1 MegOhm.

(4) Damage overload of 260 V (DC & AC r.m.s.) to 2 kHz, reducing to 10 V r.m.s. at 50 kHz and above.

(5) 50 kHz Low Pass Filter. Enabled using Special Function 11.

10 The main characteristics of INPUT B are as follows:

(1) Frequency range of 40 MHz to 1.3 GHz.

(2) BNC input connector (Fused).

(3) Input impedance of 50 Ohms.

(4) Damage overload of +29 dBm protected by the fuse inside the input connector.

11 The main characteristics of INPUT C are as follows:

(1) Frequency range of 500 MHz to 20 GHz;

(2) Input connector - Type N;

(3) Input impedance of 50 Ohms.

(4) Damage overload of +25 dBm peak.

ADDITIONAL FREQ C ACQUISITION MODES

12 (1) MANUAL - This function is used to override the automatic acquisition cycle of FREQ C. It enables the user to manually enter a center frequency and achieve the fastest possible read rates.

(2) LOW FM - When enabled this function selects an extended acquisition time to enable frequency readings of signals with low modulation rates. This function is only used during FREQ C measurements.

(3) TRACK - When enabled this function selects the fastest possible auto-acquisition cycle to enable swept-frequency readings. This function is only used during FREQ C measurements.

MATHS FUNCTIONS

13 (1) MULT - When activated this function scales readings by the factor stored in the 'MULT' store.

(2) OFFSET - When activated this function displays the difference between the measured value and the number held in the 'OFFSET' store.

(3) SMOOTH - This is a Special Function (SF 21). Selecting SMOOTH causes the counter to take a running average of the input frequency and display those digits that are stable. Place- holding zeros (in the form of half-height zeros) are used in place of unstable digits.

SPECIAL FUNCTIONS

14 SF - This function preselects special functions and enables them.

STORE/RECALL FUNCTIONS

15 (1) STORE - This function enables the operator to store data in specific stores.

(2) RECALL - This function enables the operator to recall the contents of specific stores.

(3) MHz - This function is a 10^6 multiplier, used when entering numbers into stores.

(4) +/- - This function is used to control the sign of entered numbers.

SAMPLE RATE

16 SAMPLE - This function is continuously enabled and controls the display sample rate.

ERROR INDICATION

17 Certain errors in the operation of the instrument will result in the generation of error codes which will be displayed. Details are given in Section 4 of this manual.

DISPLAY FORMAT

18 A 13 digit numeric (13 x 7 segment) display with units annunciators is used. An overflow of the most significant digit can be used to further increase the display resolution.

HOLD FEATURE

19 The Hold feature allows readings to be held indefinitely. A new measurement cycle is initiated using the RESET key.

RESOLUTION AND GATE TIME

20 The gate time is determined by the display resolution selected. Details of the relationship between gate time and display resolution for each measurement mode are given in Section 4 of this manual.

EXTERNAL FREQUENCY STANDARD INPUT

21 The instrument may be operated using an external frequency standard. The instrument will operate from the external standard, in preference to the internal standard, whenever the signal at the EXT. STD. INPUT socket is of sufficient amplitude. It will revert to operation from the internal standard automatically if the input from the external standard is removed.

STANDBY MODE

22 When the instrument is switched to standby, the internal frequency standard continues to operate and the instrument status is maintained but the measuring circuits are switched off. If the battery pack is fitted and an external power supply is connected, the battery is charged at the full rate.

INITIALIZATION

23 When the instrument is first switched on, or when it is initialized via the GPIB, it will perform the following:

(1) A software and hardware check. Error messages will be displayed if a fault is found.

(2) The display will then show the unit number for two seconds, i.e. 2101.

(3) The display will then show the software number for two seconds.

(4) The instrument will then set itself to the following state:

	FUNCTION	STATE
(a)	STANDBY/NORMAL	NORMAL
(b)	MEASUREMENT MODE	FREQ C
(c)	RESOLUTION	1 Hz
(d)	MANUAL	OFF (Store value: 1 GHz)
(e)	SF	OFF (Store value: 10, 20, 30, 40, 50, 60, 70, 80, 90)
(f)	MULT	OFF (Store value: 1)
(g)	OFFSET	OFF (Store value: 0)
(h)	SAMPLE RATE	OPTIMUM (Store value: 0)
(j)	LOW FM	OFF
(k)	TRACK	OFF
(l)	HOLD	OFF

GPIB INTERFACE

24 An internally mounted interface to the IEEE-488.2-GPIB is fitted to the instrument as standard. This permits remote control of all the instruments functions except the power ON/OFF switching and the STANDBY/CHARGING facility.

NOTE: If the instrument is ordered with a Battery Pack Option, then a GPIB is not fitted. However, the Battery Pack Option can be removed and a GPIB fitted in its place.

25 On switch-on the instrument will set itself to the following state:

(m)	LO Store (for SF41)	340 MHz
(n)	HN Store (for SF41)	-37
(o)	GPIB DUMP Mode	OFF

(p) GPIB F.P. Commands ON

(q) GPIB Enable Register 0

26 An adaptor, Racal-Dana part number 23-3254, is available as an accessory to convert the connector to the IEC 625-1 standard.

OPTIONS AVAILABLE

Frequency Standards (04X Options)

27 A wide range of internal frequency standard options is available. The technical specifications are given in Section 1 of this manual. The frequency standard can be changed, if required, by the customer: instructions are given in Section 3.

Reference Frequency Multiplier (Option 10)

28 The reference frequency multiplier is an internally-mounted, phase- locked multiplier, which permits the use of external frequency standard signals at 1 MHz, 2 MHz, 5 MHz or 10 MHz. The multiplier can be fitted by the customer: instructions are given in Section 3.

Battery Pack (Option 07)

29 Fitting the internal Battery Pack Assembly permits the instrument to be used in locations where no suitable AC supply is available. The option also allows operation from an external DC supply.

30 The battery is trickle-charged whenever the instrument is operated from an AC supply and the INTERNAL/EXTERNAL switch is at INTERNAL BATTERIES. Charging at the full rate is carried out when the instrument is switched to the standby mode and connected to an external AC or DC supply. A full charge requires approximately 14 hours.

31 The instrument will operate continuously from a fully-charged battery for approximately two hours (30 hours in standby). It will switch off automatically when the battery reaches the discharged condition. The STBY/CHRG indicator starts to flash approximately 15 minutes before this occurs. The battery life can be significantly extended by use of the Battery Save facility.

32 The Battery Pack option contains a switchable Battery Save function. When in this mode and not connected to an external supply, the instrument times out into STANDBY mode after one minute. Pressing the STBY key will return the instrument to operational mode.

33 The battery pack can be fitted by the customer: instructions are given in Section 3 (See NOTE).

NOTE: This option cannot be installed in instruments that are fitted with the GPIB Interface, without first removing the GPIB Interface from the instrument.

Rack Mounting Kits

34 The following kits permitting the instrument to be mounted in a standard 19-inch rack are available:

(1) Single instrument, fixed-mount kit (Option 60A).
(Racal-Dana part number 11-1648).
The mounted instrument occupies half the rack width and is two rack units (3.5 inches) in height. The instrument is mounted offset in the rack and may be at either side.

(2) Double instrument, fixed mount kit (Option 60B).
(Racal-Dana part number 11-1649).
The panel of the mounting kit occupies the full width of the rack and is two rack units (3.5 inches) in height.

CAUTION: TWO 2101s CANNOT BE MOUNTED SIDE-BY-SIDE. IF MOUNTING A 2101 IN A DOUBLE INSTRUMENT MOUNTING KIT, IT MUST BE MOUNTED TO THE LEFT OF THE RACK TO ALLOW FREE AIRFLOW THROUGH THE INSTRUMENT COOLING FAN.

35 All the kits can be fitted by the customer: instructions are given in Section 3.

SECTION 3 PREPARATION FOR USE

UNPACKING

1 Unpack the instrument carefully to avoid unnecessary damage to the factory packing.

2 If it becomes necessary to return the instrument to Racal-Dana Instruments for calibration or repair, the original packaging should be used. If this is not possible, a strong shipping container should be used. Ensure that sufficient internal packing is used to prevent movement of the instrument within the container during transit.

POWER SUPPLY

AC Line Voltage Setting

3 Before using the instrument, check that the AC voltage selector is set correctly for the local AC supply. The setting in use can be seen through a window in the hinged cover of the line input plug.

4 If it is necessary to change the setting, proceed as follows:

(1) Switch off the AC supply and remove the power cord.

(2) Using a 0.25 inch flat-bladed screwdriver, prise open the hinged cover.

(3) Remove the voltage setting drum.

(4) Withdraw the fuse carrier by pulling the end, marked with an arrow, straight out of the aperture.

(5) Ensure that the fuse fitted is suitable for the voltage range in use (see 'Line Fuse').

(6) Replace the fuse and carrier. Ensure the arrow on the fuse carrier points in the same direction as those on the underside of the cover.

(7) Replace the voltage setting drum so that the required setting is outermost.

(8) Close the hinged cover and ensure that the required setting is visible in the window.

(9) Reconnect the power cord.

Line Fuse

5 Check that the rating of the line fuse is suitable for the AC voltage range in use. The fuse should be of the 5 mm x 20 mm, glass cartridge, surge-resisting type. The required rating is:

90 V to 127 V: 500 mAT (Racal-Dana part number 23-0022).
193 V to 253 V: 315 mAT (Racal-Dana part number 23-0032).

Power Cord

6 The 2101 is a Safety Class 1 instrument, and is designed to meet international safety standards. A protective ground terminal, which forms part of the power-input connector on the rear panel, is provided. The instrument is provided with a three-core power cord. Only the power cord supplied should be used to make electrical connection to the power-input connector.

7 AC power for the instrument must be taken from a power outlet incorporating a protective ground connector. When the green/yellow conductor of the power cord is joined to this connector the exposed metalwork of the instrument is grounded. The continuity of the protective ground connection must not be broken by the use of two- core extension cords or three-prong to two-prong adapters.

8 Connection of the power cord to the power outlet must be made in accordance with the standard color code as follows:

AC Supply	European	American
Line	Brown	Black
Neutral	Blue	White
Ground (Earth)	Green/Yellow	Green

FUNCTIONAL CHECK

9 The functional check tests the operation of many of the instrument's circuits to establish whether the instrument is functioning correctly. The procedure should be followed when the instrument is first taken into use, and after transportation to a new location. It does not check that the instrument is operating to the published specification. Detailed specification tests are given in Section 7 of the Maintenance Manual.

10 (1) Connect the instrument to a suitable AC supply.

(2) Switch the instrument on. Check that the instrument type- number appears in the display for approximately two seconds, followed by a number which indicates the software version and issue number for approximately two seconds. The instrument will then set itself to the initialized state.

(3) Press the FUNCTION ↓ key until the CHECK indicator lights. Check that the display shows 10.000 000 00 and the GATE indicator is flashing.

(4) Press the RESOLUTION ↓ key six times, ensuring that the resolution of the display is decreased by one digit each time.

(5) Press the RESOLUTION ↑ key six times, ensuring that the display resolution of the display is increased by one digit each time.

(6) Switch the instrument off.

FREQUENCY STANDARD

11 If it is intended to use an external frequency standard, the frequency standard should be connected to the EXT. STD. INPUT connector on the rear panel of the instrument. The connection should be made using coaxial cable. Switch on the frequency standard and the instrument: check that the EXT STD indicator on the front panel of the instrument lights.

12 A 10 MHz signal, derived from the standard in use, is available at the 10 MHz STD OUTPUT connector on the rear panel of the instrument. If this signal is used, the connection should be made using coaxial cable.

PREPARATION FOR USE WITH THE GPIB

Introduction

13 The instrument must be prepared for use in accordance with the instructions given in the section titled "POWER SUPPLY" before the instructions in this section are implemented.

Connection to the GPIB

14 Connection to the GPIB is made via a standard IEEE-488 connector mounted on the rear panel. The pin assignment is given in TABLE 3.1. An adaptor, Racal-Dana part number 23-3254, to convert the connector to the IEC 625-1 standard is available as an optional accessory.

TABLE 3.1

GPIB Connector Pin Assignment

Pin	Signal Line	Pin	Signal Line
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	Gnd (6)
7	NRFD	19	Gnd (7)
8	NDAC	20	Gnd (8)
9	IFC	21	Gnd (9)
10	SRQ	22	Gnd (10)
11	ATN	23	Gnd (11)
12	SHIELD	24	Gnd (5 & 17)

Address Setting and Display

15 The interface address is set using five switches, A1 to A5, which are mounted on the rear panel. The permitted address settings, in binary, decimal and ASCII character form are given in TABLE 3.2. The GPIB address can be displayed, in decimal form, by pressing:

SHIFT RECALL LOCAL

If the address is changed, this key sequence must be repeated to display the new address. The instrument is returned to the measurement mode by pressing:

CONTINUE

16 For addressed operation, the TALK ONLY switch must be in the logic '0' position (down). When this switch is in the logic '1' position, the interface is switched to the talk-only mode. The setting of switches A1 to A5 are then irrelevant.

GPIB CHECK

17 The procedure which follows checks the ability of the instrument to accept, process and send GPIB messages. The correct functioning of the instrument under local control should be verified before the procedure is attempted.

18 The recommended test equipment is the Hewlett-Packard HP-85 GPIB controller, with the I/O ROM in the drawer. It is assumed that the select code of the controller I/O port is 7, and that the address of the instrument is 17 (to change the address see 'Address Setting and Display'). If any other controller or select code/address combination is used, the GPIB commands given in the following paragraphs will require modification. The controller should be connected to the GPIB interface of the instrument via a GPIB cable. No connection should be made to INPUTs A, B or C.

19 Successful completion of the GPIB check proves that the instrument's GPIB interface is operating correctly. The procedure does not check that all the device-dependent commands can be executed. However, if the GPIB interface works correctly and the instrument operates correctly under local control, there is a high probability that it will respond to all device-dependent commands.

Remote and Local Message Check

20 Switch the GPIB controller and instrument on. Check that the REM, ADDR and SRQ indicators flash on and off once. If the indicators do not flash, or if they flash continuously, there is a fault on the GPIB board.

21 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message true, together with the instrument's listen address.	REMOTE 717	

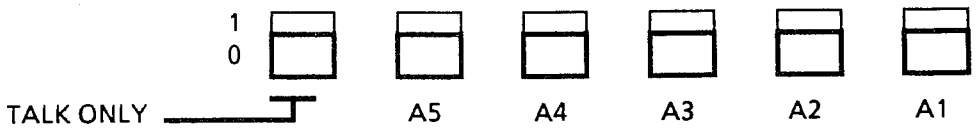
Check that the REM indicator lights.

22 Test as follows:

Action	HP-85 Code	Your Controller
Send the device dependent command CHECK.	OUTPUT 717; "CHECK"	

Check that the ADDR indicator lights and that the Check mode is selected.

TABLE 3.2
Address Switch Settings



Switch Settings					Address Codes		
A5	A4	A3	A2	A1	Decimal	ASCII Listen Address	ASCII Talk Address
0	0	0	0	0	0	SP	@
0	0	0	0	1	1	!	A
0	0	0	1	0	2	"	B
0	0	0	1	1	3	#	C
0	0	1	0	0	4	$	D
0	0	1	0	1	5	%	E
0	0	1	1	0	6	&	F
0	0	1	1	1	7	'	G
0	1	0	0	0	8	(	H
0	1	0	0	1	9	)	I
0	1	0	1	0	10	*	J
0	1	0	1	1	11	+	K
0	1	1	0	0	12	,	L
0	1	1	0	1	13	-	M
0	1	1	1	0	14	.	N
0	1	1	1	1	15	/	O
1	0	0	0	0	16	0	P
1	0	0	0	1	17	1	Q
1	0	0	0	1	18	2	R
1	0	0	1	1	19	3	S
1	0	1	0	0	20	4	T
1	0	1	0	1	21	5	U
1	0	1	1	0	22	6	V
1	0	1	1	1	23	7	W
1	1	0	0	0	24	8	X
1	1	0	0	1	25	9	Y
1	1	0	1	0	26	:	Z
1	1	0	1	1	27	;	[
1	1	1	0	0	28	<	/
1	1	1	0	1	29	=	]
1	1	1	1	0	30	>	^

Instrument shipped with this setting

23 Test as follows:

Action	HP-85 Code	Your Controller
Send the instrument's listen address followed by the GTL message.	LOCAL 717	

Check that the REM indicator is off. The ADDR indicator will also be off if the controller used sends the unlisten message (UNL) true automatically. This happens when using the HP-85.

Local Lockout and Clear Lockout Check

24 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message true, together with the instrument's listen address	REMOTE 717	
Send the LLO message	LOCAL LOCKOUT 7	

Check that the REM indicator lights. Operate the LOCAL key on the front panel and verify that the REM indicator remains lit.

25 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message false	LOCAL 7	

Check that the REM indicator is off.

6 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message true, together with the instrument's listen address	REMOTE 717	

Check that the REM indicator lights. Press the LOCAL key and verify that the REM indicator turns off.

Data Output Check

27 Test as follows:

Action	HP-85 Code	Your Controller
Set the instrument to the check mode by sending the listen address, followed by the device dependent command CHECK.	OUTPUT 717 "CHECK; MEAS?"	
Prepare a store to receive a 22 byte string.	DIM Z$ [22]	
Send the instrument's talk Address. Store the 22-byte data string in the prepared store.	ENTER 717; Z$	
Display the contents of the store.	DISP Z$	

Check that the controller displays CK+00010.00000000E+06 with the cursor moved to the next line, indicating that the line feed (LF) and END/OR Identity (EOI) have been accepted.

SRQ and Status Byte Check

28 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message true.	REMOTE 717	
Set the instrument to generate the SRQ message on receipt of a command error.	OUTPUT 717; "*ESE 32;*SRE 32"	
Set the instrument to send the SRQ message when an error is detected, and force the generation of a command error by sending the non-existent device-dependent command XXX.	OUTPUT 717; "XXX"	
Store the status of the GPIB interface of the controller, in binary form, as variable T.	STATUS 7, 2; T	
Display the status of the SRQ line.	DISP"SRQ = ";BIT (T,5)	

Check that the controller displays SRQ = 1, the SRQ status bit is at logic 1 or the SRQ line is less than or equal to 0.8 V. Check that the SRQ indicator on the instrument is lit.

29 Test as follows:

Action	HP-85 Code	Your Controller
Conduct a serial poll and store the status byte as variable R.	R = SPOLL (717)	
Display variable R.	DISP"R = "; R	

Check that the SRQ indicator is turned off when the serial poll is made. The value of R should be 91 (in binary form, R should be 01100000). If using the HP-85 controller, check that the ADDR indicator on the instrument is turned off.

IFC Check

30 Test as follows:

Action	HP-85 Code	Your Controller
Send the ATN message false	RESUME 7	
Send the IFC message false	ABORTIO 7	

Check that the ADDR indicator is turned off.

TALK ONLY Selector Test

31 (1) Set the TALK ONLY switch on the instrument rear panel to '1'. Check that the REM indicator is turned off and the ADDR indicator lights.

(2) Set the TALK ONLY switch to '0'. Check that the ADDR indicator is turned off.

OPTION FITTING INSTRUCTIONS

Single-Instrument Fixed Rack Mounting Kit 11-1648 (Option 60A)

32 The kit comprises:

Item	Qty	Racal-Dana Part Number
Short mounting bracket	1	16-0643
Long mounting bracket	1	16-0644
Screw, M4 x 16	4	24-7733
Crinkle washer M4	4	24-2802
Spacer, plain M4 x 5	4	24-4112
Screw, M6 x 16	4	24-7795
Cup washer, M6	4	24-2809
Caged nut, M6	4	24-2240

33 Assemble the kit to the instrument as follows:

(1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel; remove the bezel.

(3) Remove the bottom cover by sliding it towards the rear of the instrument.

(4) Remove the instrument's feet from the bottom cover and retain them for future use.

(5) Replace the bottom cover. Replace and secure the bezel.

(6) Remove the four blind grommets from the sides of the instrument. This will reveal two threaded holes in each side frame.

(7) At one side of the instrument, secure a mounting bracket to the side frame, using two spacers, M4 screws and crinkle washers. Position the spacers between the mounting bracket and the side frame.

(8) Repeat step (7) at the other side of the instrument.

(9) Fit the cup washers to the M6 screws. Offer the instrument up to the required position, and secure the brackets to the rack using the M6 screws and nuts.

Double-Instrument Fixed Rack Mounting Kit 11-1649 (Option 60B)

CAUTION: TWO 2101s CANNOT BE MOUNTED SIDE-BY-SIDE. IF MOUNTING A 2101 IN A DOUBLE INSTRUMENT MOUNTING KIT, IT MUST BE MOUNTED TO THE LEFT OF THE RACK TO ALLOW FREE AIRFLOW THROUGH THE INSTRUMENT COOLING FAN.

34 The kit comprises:

Item	Qty	Racal-Dana Part Number
Short mounting bracket	2	16-0643
Screw, M4 x 16	4	24-7733
Crinkle washer, M4	4	24-2802
Spacer, plain, M4 x 5	4	24-4112
Spacer, female	2	14-1583
Spacer, male	2	14-1584
Mating plate	1	13-2000
Rivet, plastic	4	24-3211
Screw, M6 x 16	4	24-7995
Cup washer, M6	4	24-2809
Caged nut, M6	4	24-2240

35 Prepare the instrument as follows:

(1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel; remove the bezel.

(3) Remove the bottom cover by sliding it towards the rear of the instrument.

(4) Remove the instrument's feet from the bottom cover and retain them for future use.

(5) Replace the bottom cover. Replace and secure the bezel.

(6) Remove the four blind grommets from the sides of the instrument. This will reveal two threaded holes in each side frame.

36 Assemble the kit to the instrument as follows:

(1) On each side of the instrument, secure a mounting bracket to the side frame, using two plain spacers, M4 screws and crinkle washers. Position the spacers between the mounting bracket and side frame.

(2) Fit the cup washers to the M6 screws. Offer the instrument up to the rack in the left-hand position, and secure the brackets to the rack using the M6 screws and nuts.

Temperature Compensated Frequency Standard, 11-1713 (Option 04T)

37 The kit comprises:

Item	Qty	Racal-Dana Part Number
Plate assembly	1	11-1610
Oscillator PCB	1	19-1208
Crinkle washer, M3	3	24-2801
Screw, M3 x 6	3	24-7721

Installation

38 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel; remove the bezel.

(3) Remove the four blind grommets from the sides of the instrument.

(4) Remove the top cover by sliding it towards the rear of the instrument.

(5) Remove the frequency standard already fitted. Instructions are given in this chapter, according to type.

(6) Secure the PCB to the plate assembly, using an M3 screw and washer from the kit. The screw should be passed through the mounting hole in the board and screwed into the threaded spacer of the plate assembly. The component side of the board should be towards the plate assembly.

(7) Connect the PCB to the motherboard at PL14, with the plate assembly towards the rear panel of the instrument.

(8) Secure the plate assembly to the rear panel, using two M3 screws and washers. The screws pass through the holes adjacent to FREQ. STD. ADJUST aperture and screw into the plate assembly.

(9) Replace the top cover. Replace the four blind grommets. Replace and secure the bezel.

Removal

39 (1) Remove the two screws adjacent to the FREQ. STD. ADJUST aperture in the rear panel.

(2) Pull the PCB and plate assembly upwards until the board is disconnected from the motherboard.

Ovened Frequency Standards 11-1710 and 11-1711 (Options 04A and 04B)

40 The kit comprises:

Item	Qty	Racal-Dana Part Number
Oscillator assembly	1	9444 for 11-1710 9423 for 11-1711
Crinkle washer, M3	2	24-2801
Screw, M3 x 6	2	24-7721

Installation

41 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel; remove the bezel.

(3) Remove the four blind grommets from the sides of the instrument.

(4) Remove the top cover by sliding it towards the rear of the instrument.

(5) Remove the frequency standard already fitted. Instructions are given in this chapter, according to type.

(6) Connect the flying lead on the oscillator assembly to PL14 on the motherboard.

(7) Secure the oscillator assembly to the rear panel of the instruments, using the M3 screws and washers. The screws pass through the holes adjacent to the FREQ. STD. ADJUST aperture and screw into the oscillator assembly.

(8) Replace the top cover. Replace the blind grommets. Replace and secure the bezel.

Removal

42 (1) Remove the two screws adjacent to the FREQ. STD. ADJUST aperture in the rear panel.

(2) Lift the oscillator assembly out of the chassis and disconnect the flying lead from the motherboard at PL14.

Reference Frequency Multiplier Option 11-1645 (Option 10)

43 The kit comprises:

Item	Qty	Racal-Dana Part Number
Frequency multiplier	1	19-1164
Crinkle washer, M3	2	24-2801
Screw, M3 x 6	2	24-7721

Installation

44 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel; remove the bezel.

(3) Remove the four blind grommets from the sides of the instrument.

(4) Remove the top cover by sliding it towards the rear of the instrument.

(5) Remove the frequency standard if an ovened type is fitted.

(6) Remove the shorting links between pins 5 and 6 and pins 8 and 9 on PL16.

NOTE: These links should be stored in a safe place. They must be replaced if Option 10 is removed from the instrument.

(7) Connect the frequency multiplier PCB to the motherboard at PL16 and PL17, with the threaded spacers towards the right- hand side frame.

(8) Secure the PCB to the side frame, using the M3 screws and washers.

(9) Replace and secure the frequency standard if it was removed in (5).

(10)Replace the top cover. Replace the blind grommets. Replace and secure the bezel.

Battery Pack Option 11-9009 (Option 07)

45 The kit comprises:

Item	Qty	Racal-Dana Part Number
PCB assembly	1	11-7051
Mounting bracket	1	11-1599
Battery pack	1	11-1723
Cover plate	1	13-2040
Crinkle washers, M3	2	24-2801
Screws, M3 x 6	2	24-7721
Crinkle washers, M4	2	24-2802
Screws, M4 x 8	2	24-7730
Plain washers, M4	6	24-2705
Spare fuse, 3A	1	24-0069
Cup Washer, nylon	4	24-2816
Screw, M4 x 10 C'sk	4	24-7543
Plain washer, M3	3	24-2703
Handles	2	15-0771
Screws, M4 x 12 Pan Head	4	24-7732
Insert	2	13-2060

NOTE: This option cannot be fitted to an instrument already fitted with the GPIB interface without first removing the GPIB interface.

Installation

46 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel; remove the bezel.

(3) Remove the four blind grommets from the sides of the instrument.

(4) Remove the top cover by sliding it towards the rear of the instrument.

(5) (a) Remove the blanking plate from the rear panel by pushing out the rivets from the inside of the instrument.

OR

(b) Remove the GPIB assembly, if fitted, see Section 7 of the Maintenance Manual.

(6) Hold the PCB assembly with the switches to the rear of the instrument and the PCB connector pointing downwards.

(7) Carefully lower the assembly into the chassis, guiding the switches through the rear panel and connect the PCB to the motherboard at PL21, taking care that it mates correctly.

(8) Position the cover plate over the switches protruding through the rear panel and secure using the M3 screws and washers.

(9) Fit the mounting bracket to the side frame, using two M4 x 10 countersunk screws, cup washers and plain washers.

(10) With the flying lead towards the rear of the instrument, carefully lower the battery pack into the instrument, ensuring that the lower left hand lug passes through the aperture in the heatsink/sidepanel. Also check that the upper right hand supporting lug rests on the mounting bracket.

(11) Secure the battery pack to the left-hand side frame using two M4 x 10 countersunk screws, cup washers and plain washers. Secure the right-hand supporting lugs to the mounting bracket using M4 screws, plain and crinkle washers.

(12) Connect the flying lead on the battery pack to the connector on the PCB assembly.

(13) Replace the top cover. Replace the blind grommets. Replace and secure the bezel.

(14) Fit the handles, using the M4 x 12 screws. Fit the self adhesive inserts.

Power Limiter Option 17-1103 (Option 11)

47 The kit comprises:

Item	Qty	Racal-Dana Part Number
Power Limiter	1	17-1103

Installation

48 (1) Remove the instrument top cover and the module stack as described in Section 7 of the Maintenance Manual.

NOTE: The coaxial and ribbon connectors do not have to be removed from the module stack. Carefully place the module stack on top of the GPIB board.

(2) Remove the Sampler Module as described in Section 7 of the Maintenance Manual.

(3) Loosen Channel C ring nut and retighten finger-tight only.

(4) Connect the Power Limiter to the Sampler Bracket connector with the Limiter main label facing away from the bracket.

(5) Connect the Sampler to the Power Limiter and secure the connector finger-tight only.

(6) Refit the Sampler to the bracket with the retaining screws finger-tight only.

(7) Tighten the SMA connector to 1 Nm using the SMA torque wrench. Fully tighten Channel C ring nut and tighten the Sampler Module securing screws.

(8) Replace the complete assembly in the instrument. Reconnect PL32 and 36 to the Sampler Module.

(9) Reconnect SK15 to PL15 on the motherboard.

(10) Replace the ring nut on the Input C connector.

(11) Replace the Module Stack ensuring the coaxial cables are located correctly.

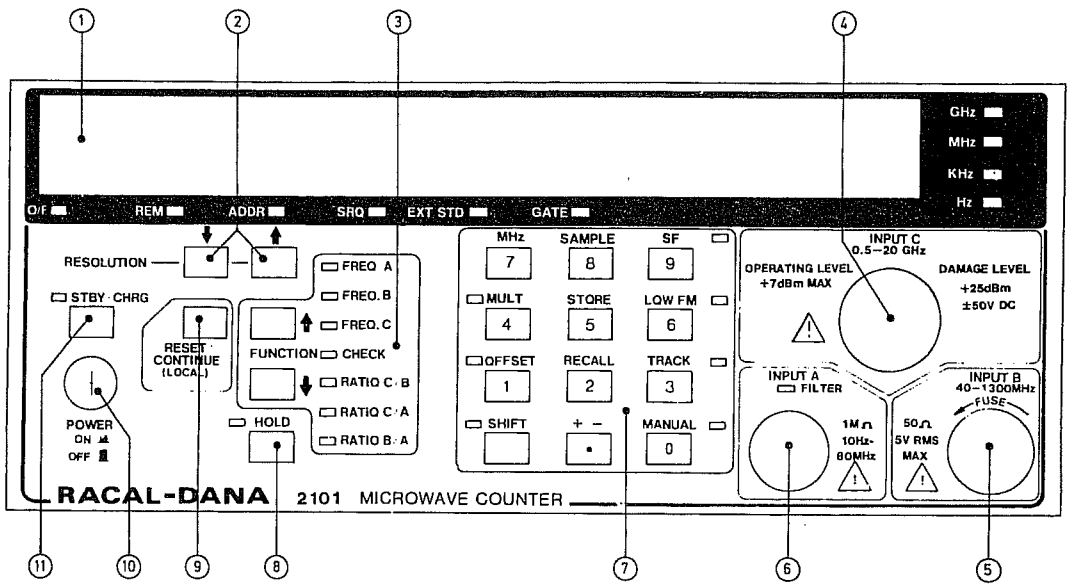
(12) Refit the top cover and rear panel bezel. Refit the bungs or the handles if previously fitted.

(13) Fit the option label to the serial number label on the instrument.

SECTION 4 OPERATING INSTRUCTIONS

INTRODUCTION

1 The instrument should be prepared for use in accordance with the instructions given in Section 3. If the instrument is being used for the first time, or at a new location, pay particular attention to the setting of the AC voltage selector and the fuse rating.



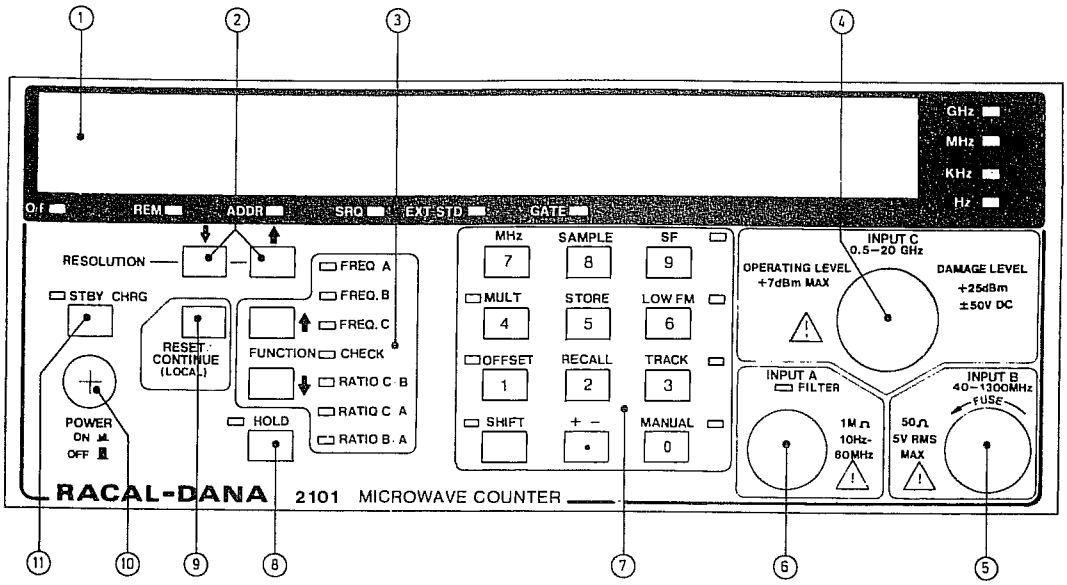
DESCRIPTION OF CONTROLS, INDICATORS AND CONNECTORS

Front Panel Items

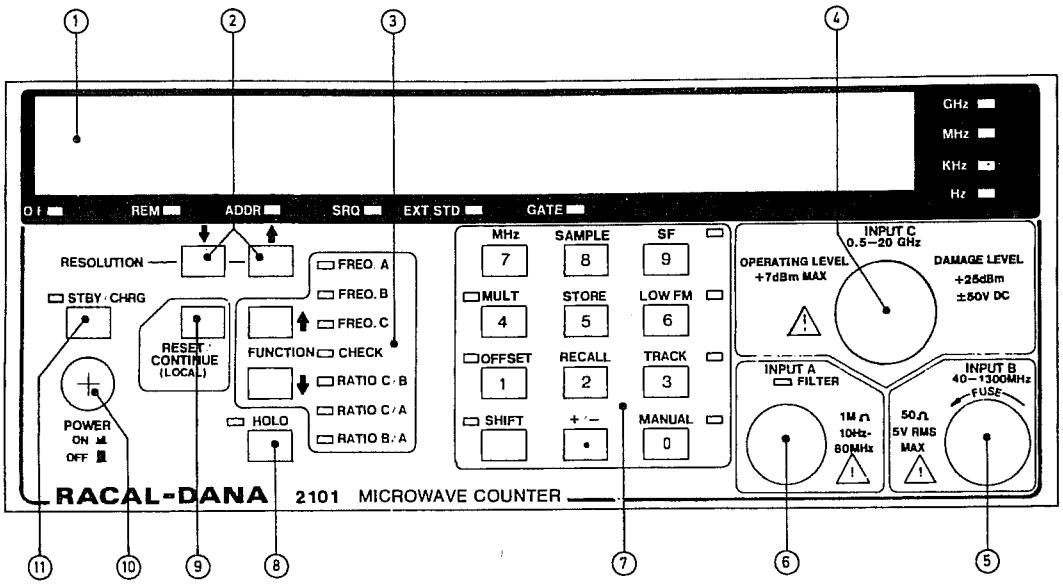
2

Reference	Item	Description
(1)	Display	A 13-digit LED display, used to display: (1) The result of a measurement. (2) A number awaiting entry into an internal store. (3) A number recalled from an internal store. (4) Error indication.

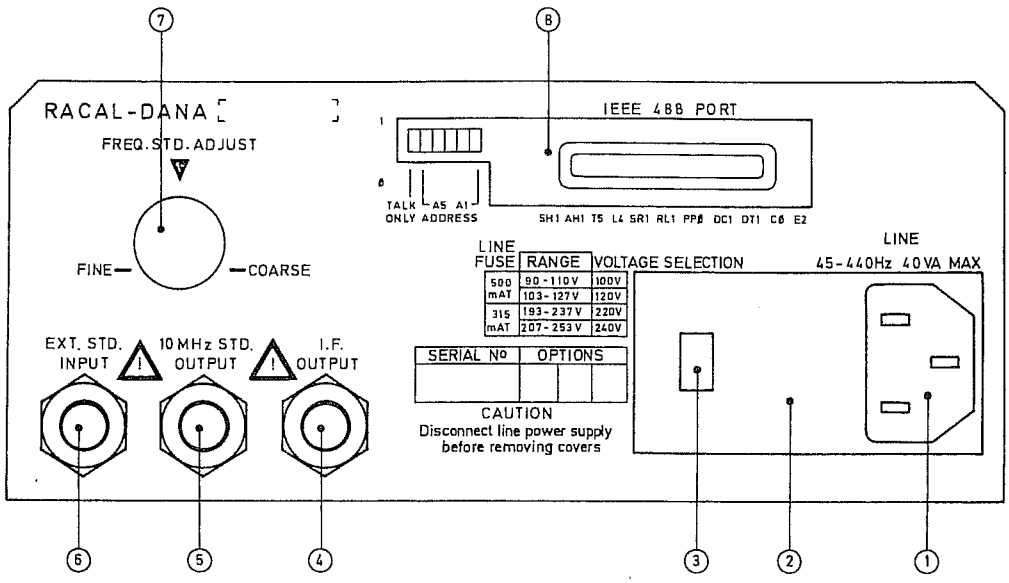
Reference	Item	Description
	O/F Indicator	Lights when the measurement result has overflowed the most significant digit of the display.
	REM Indicator	Lights when the instrument is operating under remote control.
	ADDR Indicator	Lights when the instrument is acting as a listener or a talker.
	SRQ Indicator	Lights when the instrument generates a service request.
	EXT STD Indicator	Lights when the instrument is operating from an external frequency standard.
	GATE Indicator	Lights while a measurement cycle is in progress.
	Display Units Indicators	Four indicators show the scale of the display in terms of frequency.
(2)	Resolution Control Keys	Used to step the display resolution up or down as shown by the arrows.
(3)	Function Selector	The primary measurement functions can be selected in turn using the arrowed FUNCTION keys. The function selection 'wraps round' at both ends.
(4)	INPUT C Connector	Precision N female type connector for inputs from 500MHz to 20GHz.
(5)	INPUT B Connector	BNC female fused connector for inputs from 40 MHz to 1.3 GHz.
(6)	INPUT A Connector	BNC female connector for inputs from 10 Hz to 80 MHz.



Reference	Item	Description
(7)	Numeric Keypad	Used to enter numbers into, and recall numbers from, the instrument's internal stores. Also used to enable and disable the math functions, the special functions, and to select alternate FREQ.C acquisition modes.
(8)	HOLD Key and Indicator	Successive operations put the instrument into and out of the Hold (single-shot meaurement) mode. The indicator lights when the instrument is in the Hold mode. Readings are triggered using the RESET key.
(9)	RESET/CONTINUE (LOCAL) Key	This key has three functions: RESET Clears the display and triggers a new measurement cycle when the instrument is in the measurement mode. CONTINUE Returns the instrument to the measurement mode and triggers a measurement cycle. It can also be used to clear the OP Er indication. LOCAL Returns the instrument to local control fromr emote GPIB control provided local lockout is not set.



Reference	Item	Description
(10)	POWER Switch	Controls the AC or DC power to the instrument.
(11)	STBY/CHRG Key and Indicator	Successive operations switch the instrument into and out of the standby state. The indicator lights when the instrument is in the standby state. If the Battery Pack option is installed the indicator flashes when the battery approaches the discharged state. the battery is charged at the full rate when the instrument is in standby and external power is applied.

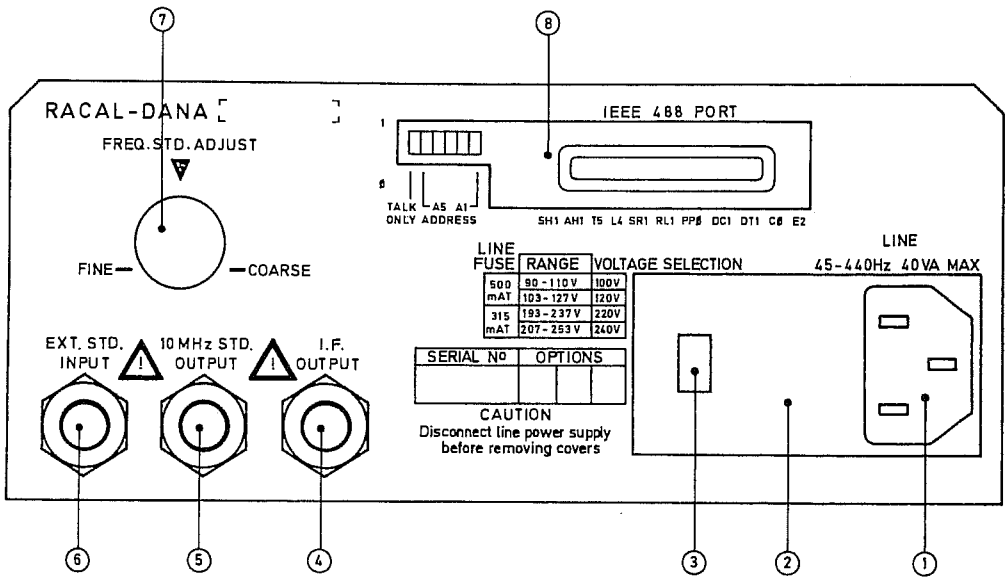


Rear Panel Items

3

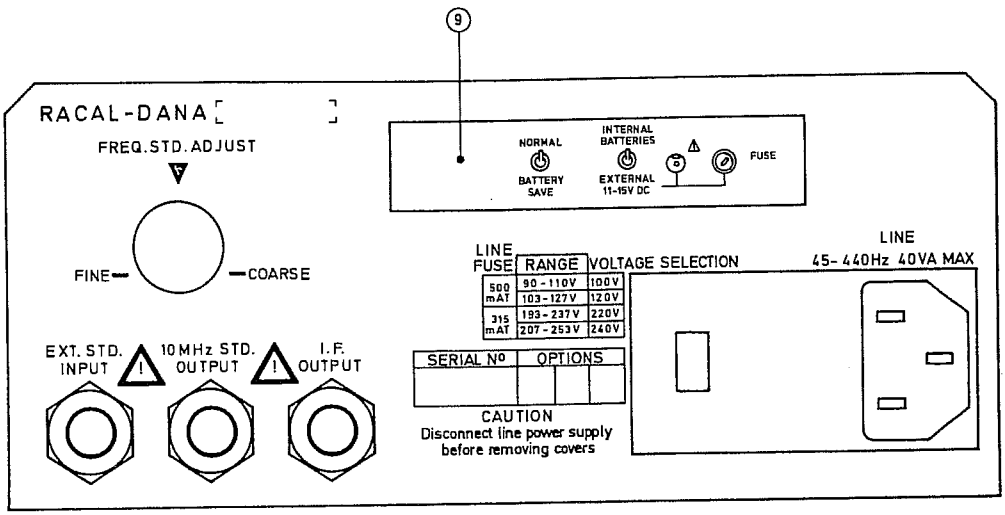
Reference	Item	Description
(1)	AC Power Input Plug (See NOTE)	A standard connector for the AC power supply. A RFI filter is incorporated.
(2)	Line Fuse (See NOTE)	A 5mm x 20mm, surge-resistant, glass cartridges fuse, located under a hinged cover next to the AC supply plug. The required fuse ratings for different line voltage ranges are shown on the panel and in Section 3 of this manual.
(3)	Line Voltage Selector (See NOTE)	Voltage selection is changed by repositioning a small drum under a hinged cover next to the AC supply plug.

NOTE: Items 1, 2 and 3 are all incorporated in one Schaffner connector unit.

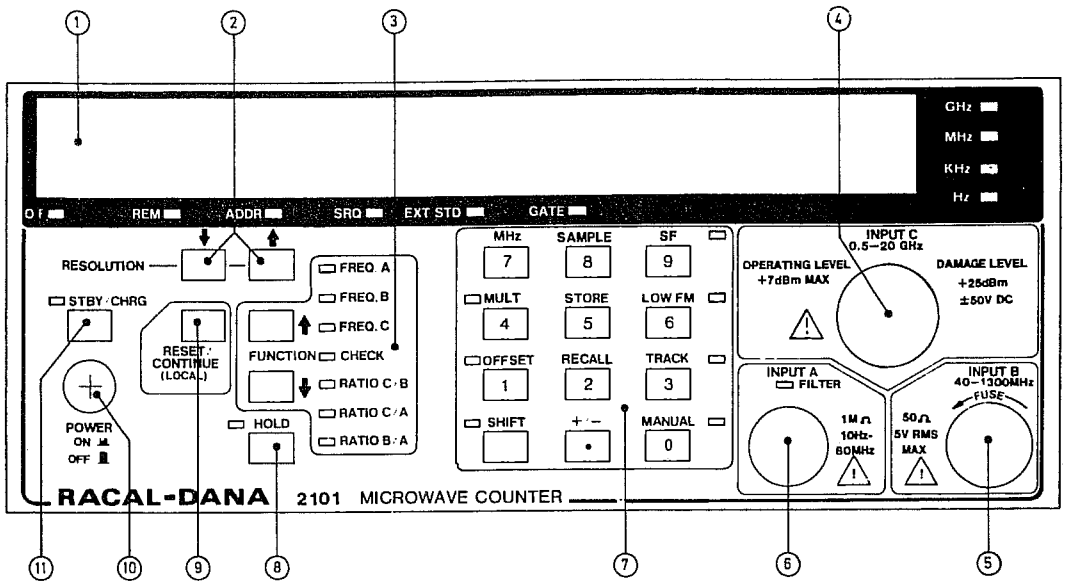


Reference	Item	Description
(4)	I.F. OUTPUT	A BNC female connector, providing an I.F. output when making measurements onINPUT C. Output is continuously available in manual operation. In automatic operation the output is available during the gate time.
(5)	10 MHz STD OUTPUT	A BNC female connector, providing a 10 MHz signal locked to the frequency standard in use.
(6)	EXT. STD. INPUT	A BNC female connector for connecting an external frequency standard input. The frequency required is 10MHz unless the reference frequency multiplier option is fitted. With this option, frequencies of 1 MHz, 2 MHz, 5 MHz and 10 MHz may be used.

Reference	Item	Description
(7)	FREQ. STD. ADJUST	This aperture provides access to allow adjustment of the internal frequency standard.
(8)	GPIB Interface	
	GPIB Address Switches	Switches A1 to A5 define the listen and talk addresses for GPIB operation in the addressed mode. The talk-only switch must be in the '0' position. With the talk-only switch in the 'I' position the instrument is set to the talk-only condition. The positions of switches A1 to A5 are then irrelevant.
	GPIB Connector	An IEEE-488-1978 std. connector used to connect the instrument to the GPIB. An adaptor, Racal-Dana part number 23-3254, to convert the connector to theIEC 625-1 standard is available as an accessory.



Reference	Item	Description
(9)	Battery-pack option	
	External DC Input	Permits the instrument power to be derived from an external fused DC supply.
	NORMAL/BATTERY SAVE Switch	Used to select the Battery-Save function.
	INTERNAL/EXTERNAL DC Supply Switch	Used to select operation from the internal battery or an external DC supply.
	DC Supply Fuse	A 0.25 x 1.25 inch glass cartridge fuse of the surge-resistant type. The required rating is 3 AT.



FREQUENCY MEASUREMENT - INPUT A

4 (1) Press the POWER switch (10) to switch on.

(2) Select FREQ A using the FUNCTION keys (3).

(3) Select the required display resolution, using the RESOLUTION keys (2).

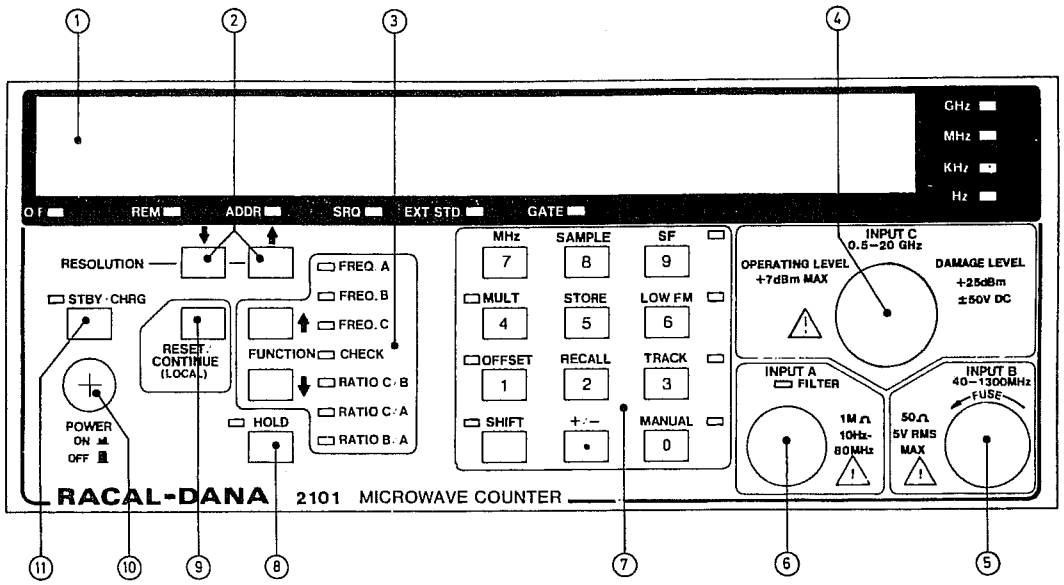
NOTE: Gate time is related to the resolution selected.

(4) If a frequency below 50 kHz is to be measured in the presence of HF noise, select the low-pass input filter by selecting special function SF 11 (see 'SPECIAL FUNCTIONS' in this Section of the Manual). Ensure that the FILTER indicator lights.

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT SIGNAL LEVEL DOES NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

(5) Connect the signal to be measured to INPUT A (6).

(6) If HOLD mode operation is required, select HOLD (8). To take a measurement, press the RESET key (9) Check that the GATE indicator lights during the measurement period. To return to the continuous measurement mode, press the HOLD key (8) again.



FREQUENCY MEASUREMENT - INPUT B

5 (1) Press the POWER switch (10) to switch on.

(2) Select FREQ B using the FUNCTION keys (3).

(3) Select the required display resolution, using the RESOLUTION keys (2).

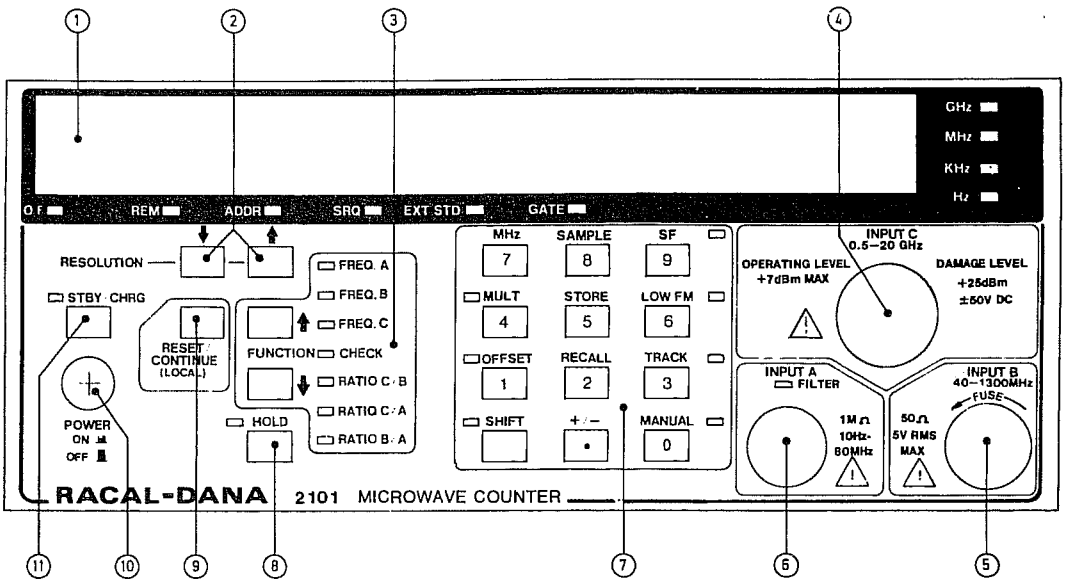
Note: Gate time is related to the resolution selected.

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT SIGNAL LEVEL DOES NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

NOTE: INPUT B is fused, see SECTION 1 of this manual.

(4) Connect the signal to be measured to INPUT B (5).

(5) If HOLD mode operation is required, select HOLD (8). To take a measurement, press the RESET key (9). Check that the GATE indicator lights during the measurement period. To return to the continuous measurement mode, press the HOLD key (8) again.



FREQUENCY MEASUREMENT - INPUT C

Normal Automatic Mode

6 (1) Press the POWER switch (10) to switch on.

(2) Select FREQ C using the FUNCTION keys (3)

(3) Select the required display resolution, using the RESOLUTION keys (2).

NOTE: Gate time is related to the resolution selected and the input frequency.

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT SIGNAL LEVEL DOES NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

(4) Connect the signal to be measured to INPUT C (4).

(5) If HOLD mode operation is required, select HOLD (8). To take a measurement, press the RESET key (9). Check that the GATE indicator lights during the measurement period. To return to the continuous measurement mode, press the HOLD key (8) again.

Manual Mode

7 In this mode the measured frequency, or a keyboard entered frequency value, is entered into the MANUAL Store, then MANUAL Mode is then selected.

8 (1) To store a center frequency (the example shows 19 GHz), press:

[1] [9] [0] [0] [0] [SHIFT] [MHz] [STORE] [MANUAL]

(2) To store the frequency shown in the display press:

[SHIFT] [STORE] [MANUAL]

(3) If Manual Mode was previously selected the new entered value of frequency is used immediately, otherwise, to enable Manual Mode press:

[SHIFT] [MANUAL]

Further Functions in FREQ C (Automatic Mode Only)

9 In FREQ C, normal AUTOMATIC Mode, two more (shifted) functions are available, these are LOW FM and TRACK.

NOTE 1:
These functions are not available in MANUAL Mode.

NOTE 2:
LOW FM and TRACK functions are mutually exclusive; only one of the functions being available at a time.

10 Selection of one function (e.g. TRACK), whilst the other function (LOW FM) is in use, will switch off the previously used function (LOW FM). Switching off the last used function (TRACK) will then return the instrument to AUTOMATIC Mode, NOT the previously used function.

Set LOW FM (FREQ C)

11 This function utilizes longer gate times to accommodate signals with low modulation rates.

12 To use this function proceed as follows:

(1) Proceed as described in 'FREQUENCY MEASUREMENT - INPUT C'.

(2) Press:

[SHIFT] [LOW FM]

The LOW FM indicator lights.

(3) To exit, press:

SHIFT LOW FM

The LOW FM indicator goes out.

Set TRACK (FREQ C)

13 This function enables the instrument to measure and display swept frequencies.

14 To use this function proceed as follows:

(1) Proceed as described in 'FREQUENCY MEASUREMENT - INPUT C'.

(2) Press:

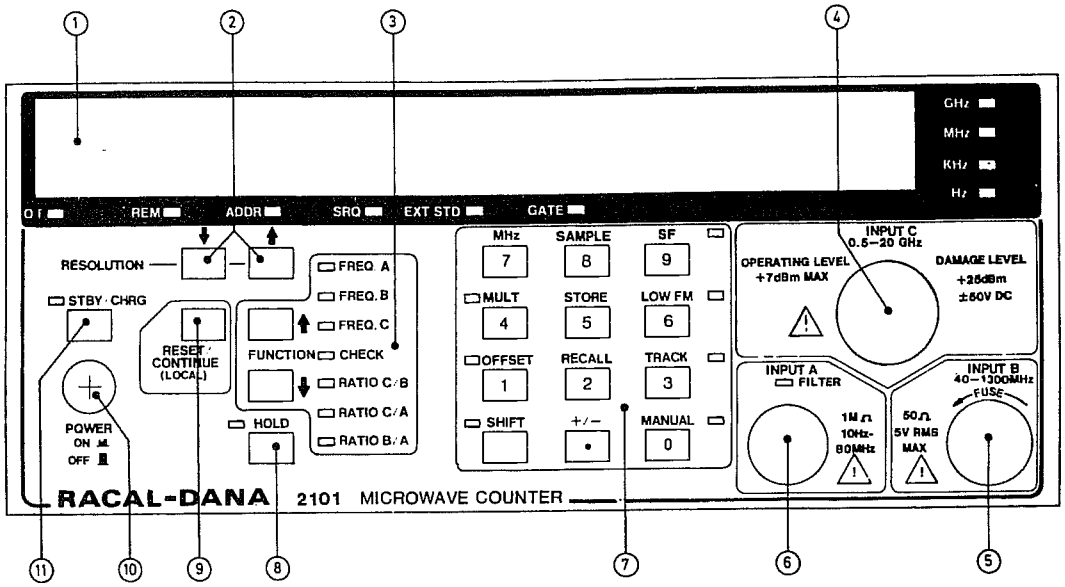
SHIFT TRACK

The TRACK indicator lights.

(3) To exit, press:

SHIFT TRACK

The TRACK indicator goes out.



RATIO MEASUREMENTS C/B, C/A AND B/A

15 These three Ratio Modes use a 'software' ratio method, whereby the denominator is sampled first, followed by the numerator. The microprocessor in the instrument then computes the ratio and displays the result.

16 For certain specific applications a 'hardware' version of RATIO B/A is available by enabling Special Function 91. This allows 'real time' ratio measurements to be made.

17 (1) Press the POWER switch (10) to switch on.

(2) Select the relevant RATIO function using the FUNCTION keys (3).

(3) Select the required display resolution, using the RESOLUTION keys (2).

(4) If INPUT A is being used for a frequency below 50 kHz in the presence of HF noise, select the Low Pass Input Filter (SF 11).

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT SIGNAL LEVEL DOES NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

NOTE: INPUT B is fused, see SECTION 1 of this manual.

(5) If hold mode operation is required, select HOLD (8). To take a measurement, press the RESET key (9). Check that the GATE indicator lights during the measurement period. To return to the continuous measurement mode, press the HOLD key (8) again.

SAMPLE RATE

18 On initial switch-on the instrument will sample signals at the highest rate (time interval between readings is ∅). However, the user can slow the sample rate down using the SAMPLE function. This sets the time interval between readings (hold time) and hence controls the sample rate.

Setting and Using the Sample Rate

19 To alter the sample rate, proceed as follows:

(1) Enter the display time required (e.g. for 100 mSec enter 0.1), using the keypad (7).

(2) Press:

SHIFT | STORE | SAMPLE

This enters the reading hold time into the SAMPLE register and is used immediately.

Displaying the Sample Rate

20 To display the reading hold time in use, press:

SHIFT | RECALL | SAMPLE

The sample rate is shown in the display.

21 To return to measurement mode, press the RESET key (9).

MULT FUNCTION

22 This function is used to display the input signal multiplied by the number held in the MULT (Multiply) register. This function can be used, for instance, to display the true frequency reading of a signal source that has been divided or multiplied before being sampled by the instrument.

Setting the Multiplier

23 To store a multiplier for later use, proceed as follows:

(1) Enter the number of the multiplier required, using the keypad (7).

(2) Press:

SHIFT | STORE | MULT

This enters the multiplier into the MULT register for future use.

Enabling the Multiplier

24 To enable the stored multiplier, press:

SHIFT MULT

The MULT indicator lights. The instrument displays the input signal scaled by the value held in the MULT store.

25 To exit this function, press:

SHIFT MULT

The MULT indicator goes out.

Displaying the Multiplier

26 If necessary the stored multiplier can be displayed by pressing:

SHIFT RECALL MULT

The multiplier is shown in the display.

27 To return to measurement mode, press the RESET key (9).

OFFSET FUNCTION

28 This function can be used to add or subtract a value to the measured frequency. It is also used to subtract the displayed frequency (nulling) to view drift or offset. For example: measuring the IF of a radio receiver, after entering the receiver local oscillator frequency as a positive offset, enables the true input frequency to be displayed.

Setting the Offset

29 If enabled, the offset frequency entered is normally subtracted from the measured signal frequency. The sign of the offset can be altered at any point during number entry by pressing:

SHIFT +/-

To store the offset frequency, proceed as follows:

(1) To enter an offset frequency (this example shows 10.5 MHz), press:

1 0 . 5 SHIFT MHz STORE OFFSET

This enters the offset frequency into the OFFSET register.

(2) To enter the displayed frequency as an offset, press:

SHIFT OFFSET

Enabling the Offset

30 To enable the stored offset, press:

SHIFT OFFSET

The OFFSET indicator lights. The instrument displays the input minus the value held in the OFFSET register.

31 To exit this function, press:

SHIFT OFFSET

The OFFSET indicator goes out.

Displaying the Offset

32 To display the stored offset, press:

SHIFT RECALL OFFSET

The offset is shown in the display.

33 To return to measurement mode, press the RESET key (9).

SMOOTH FUNCTION (SPECIAL FUNCTION 21)

34 This is Special Function 21 (see 'SPECIAL FUNCTIONS' in this Section of the Manual). Selecting SMOOTH enables the instrument to take a 'running average' of the input frequency and display those digits that are stable.

DISPLAY RESOLUTION

35 Resolution, in this context, refers to the number of zeros displayed after pressing RESET with no signal applied at an input. The resolution can be set to display from three to 10 decimal places. A 10% overrange of the display is permitted without a change of range. Because of this, an additional digit with a value of 1 is allowed at the more significant end of the display when measurements are made. With a resolution of 10 selected, the presence of this extra digit may result in the overflow (O/F) indicator being lit (FREQ C only, resolution of 0.1 Hz).

36 The resolution is changed using the arrowed resolution keys. To step up from nine to ten digits, the step-up key must be held for about two seconds.

37 With hardware RATIO B/A (SF 91) selected, no more than seven digits (plus a possible overrange) are displayed, regardless of the resolution selected.

GATE TIME

38 For INPUTs A and B, Gate Time is related to the resolution selected, as shown in TABLE 4.1a.

TABLE 4.1a

Gate Times for FREQUENCIES A and B

Number of digits in FREQ A, FREQ B & CHECK	Gate Time	Resolution Number
10	20 s	10
9	1 s	9
8	100 ms	8
7	10 ms	7
6	1 ms	6
5	1 ms	5
4	1 ms	4
3	1 ms	3

39 For INPUT C, Gate Time is related to both the resolution selected and the input frequency, as shown in TABLE 4.1b.

TABLE 4.1b

Gate Times for FREQUENCY C

Frequency GHz	Resolution			
	1 Hz	10 Hz	100 Hz	1 kHz
0.5 - 1.0	100 ms	10 ms	1 ms	1 ms
1.0 - 4.0	200 ms	20 ms	2 ms	1 ms
4.0 - 8.0	400 ms	40 ms	4 ms	1 ms
8.0 - 12.0	600 ms	60 ms	6 ms	1 ms
12.0 - 16.0	800 ms	80 ms	8 ms	1 ms
16.0 - 20.0	1 s	100 ms	10 ms	1 ms

SPECIAL FUNCTIONS

40 The special functions provided for use by the operator are listed in TABLE 4.2 Major Special Functions, and TABLE 4.3 Minor Special Functions. The major functions are those most commonly used by the operator. Each special function is defined by a two-digit number.

TABLE 4.2

Major Special Functions

Function	Code
Deselects Channel filter	10
Selects Channel A filter	11
Cancels Smooth function	20
Selects Smooth function (See NOTE 1)	21
Leading (function) letters in O/P string	80
No leading (function) letters in O/P string	81
Cancels group 90 special functions	90
Enables hardware ratio B/A	91

Setting the Special Function Register

41 When a special function is to be used, its number must first be entered into the register. To do this press:

[N] [N] [SHIFT] [STORE] [SF]

Where N N is the special function number to be entered. The digits enter the display as the keys are pressed. The instrument returns to the measurement mode automatically once the number is stored.

42 When a number is stored, it overwrites the previously stored number in the same decade. To remove a number from the register, another number must be stored.

43 The numbers in the register are retained while the instrument is switched to the standby mode.

Enabling and Disabling the Special Functions

44 The group of special functions whose numbers are entered in the special function register are enabled and disabled by pressing:

[SHIFT] [SF]

The SF indicator is lit when special functions are enabled.

TABLE 4.3

Minor Special Functions

Function	Code
Cancels all group 30 special functions	30
Displays Local Oscillator Value (See NOTE 2)	31
Displays Intermediate Frequency (See NOTE 3)	32
Displays Harmonic Number as an integer (See NOTE 3)	33
Displays Harmonic Number with fractional part (See NOTE 3)	34
Displays IF Detector Status (See NOTEs 3 & 4)	35
Displays IF Filter Status (See NOTEs 3 & 4)	36
Displays LO Detector Line Status	37
Cancels all group 40 special functions	40
Allows setting of LO & Harmonic Number (See NOTEs 3 & 5)	41
Switches LO Off under all conditions	42
Disables IF output under all conditions	43
Cancels all group 50 special functions	50
Ignore IF level detector	51
Cancels all group 70 special functions	70
Initiates front panel display checks	71
These codes are reserved for diagnostic purposes and are described in the Maintenance Manual (See NOTE 6)	72 73 74 75

NOTE 1: This function does not operate on diagnostic special functions.

NOTE 2: This function only operates during INPUT C measurements and displays the value of Local Oscillator used to make a measurement.

NOTE 3: Operates under same conditions as Special Function 31.

NOTE 4: '0' displayed = Facility Not Present.
'1' displayed = Facility Present.
(Special Function 41 must also be active).

NOTE 5: MANUAL LED is on, LO and Harmonic Number (HN) register both active. To access LO use TRACK key, to access HN use LOW FM key.

NOTE 6: Special Functions 71 to 75 can be entered into the special functions register at any time. They are active only when the instrument is in Check Mode.

45 The default state corresponds to the default state of the special function register, i.e., with special functions 10, 20, 30, 40, 50, 60, 70, 80 and 90 enabled.

NOTE: A special function entered in the register while the special functions are enabled will be enabled immediately.

To recall Special Function Register

46 One special function from each decade is entered into a special function register. Only the second digit is stored; the decade is indicated by the position of the digit in the register. The default state is with 0 entered in each position.

47 To display the contents of the register press:

SHIFT RECALL SF

A typical display is shown in Fig. 4.1.

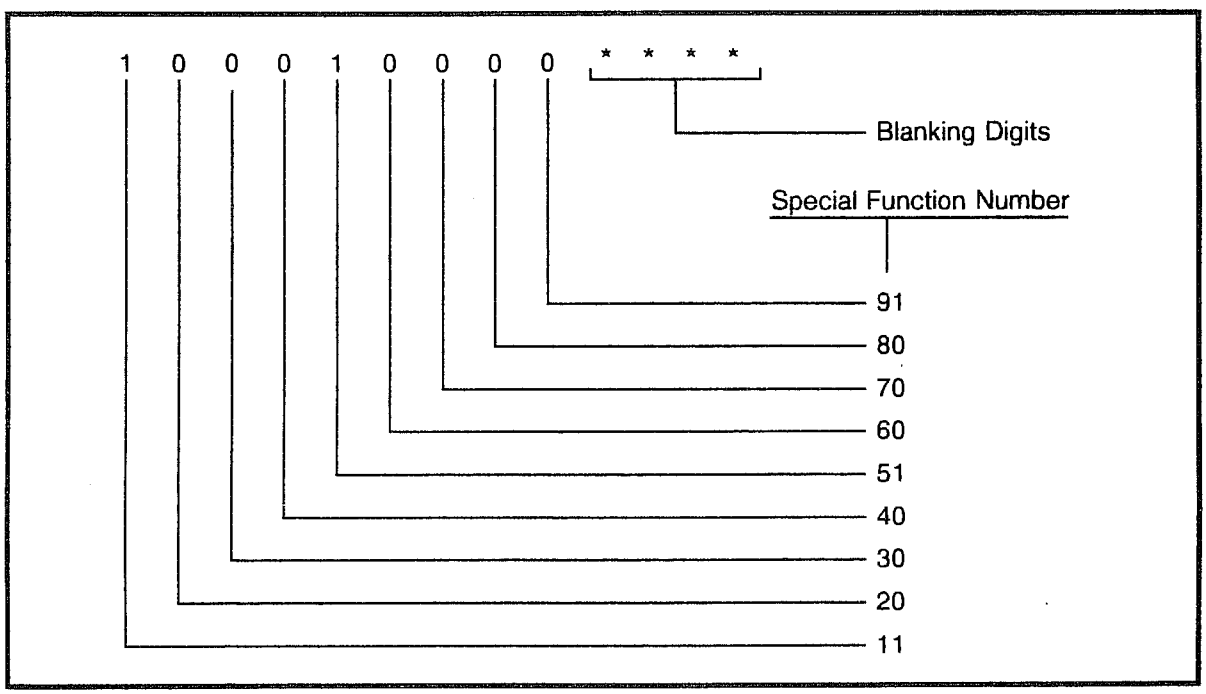


Fig. 4.1 Special Function Register Display

ERROR CODES

48 The instrument is able to detect a number of error states, which are indicated on the display. The meanings of the error codes are shown in Table 4.4.

TABLE 4.4

Error Codes

Display	Error
Op Er	Operator error caused by 'illegal' entries or attempt to enter a value out of range.
Er 02	Measurement result too large, or small, for display.
Er 03	Overfolw of internal counters.
Er 50	Incorrect result obtained when in check mode.
Er 51	Local oscillator out of lock.
Er 60	EPROM paging failure.
Er 61	RAM failure.

Clearing the Error Codes

49 Error codes are cleared as follows:

(1) Op Er, Er 02 and Er 03: Press RESET/CONTINUE (Local) key and select another measurement function.

(2) Er 50, Er 51, Er 60 and Er 61: These are equipment failure errors, switch off instrument and return it for repair.

USING THE BATTERY PACK OPTION

WARNING: LETHAL VOLTAGE
IF MEASUREMENTS ARE MADE ON SIGNAL SOURCES AT VOLTAGES GREATER THAN 50 V DC WITH THE INSTRUMENT POWERED FROM THE INTERNAL BATTERY OR AN EXTERNAL DC SUPPLY, THE GROUND CONNECTOR OF THE AC POWER SUPPLY INPUT ON THE INSTRUMENT MUST BE CONNECTED TO GROUND.

Power Supply Changeover

50 When the battery pack option is installed, the instrument can be powered from the internal battery, an external DC supply of 11 V to 16 V, or an external AC supply. If the instrument is operating from either the external DC supply or the battery, it will automatically change to operation from the AC supply when this is connected. To prevent accidental battery discharge, the battery will not take over from either the AC or external DC supply if that supply fails. An external DC supply will not take over from the AC supply if the AC supply fails.

Battery-Low Indication

51 When the instrument is working from the internal battery, or from an external DC supply, the STBY/CHRG indicator will start to flash as the supply voltage approaches the minimum permissible level. This occurs regardless of whether the instrument is in the standby mode or not. When operating from the battery, the instrument can be used in the measurement mode for approximately 10 minutes after the indicator commences flashing.

52 When the voltage of the battery or external DC supply reaches the minimum permissible level, the instrument shuts down completely.

Operating Instructions

53 Instructions for preparing the instrument to make measurements are given in the following paragraphs. No other change in the operating procedure is required.

Operating From the Battery

54 (1) Set the INT/EXT switch on the rear panel to INT.

(2) Set the BATTERY SAVE/NORMAL switch to NORMAL.

(3) Switch the instrument on.

(4) Check that the instrument goes through the normal switch-on sequence. If the STBY indicator is flashing, or if there is no display, charge the battery.

55 It is recommended that the Battery-Save facility should be used whenever possible. To select this set the BATTERY SAVE/NORMAL switch to BATTERY SAVE. The instrument will remain in the measurement mode for a predetermined period and will then switch to

standby. It can be returned to the measurement mode for the same period by pressing the STBY/CHRG key.

Operation From an External DC Supply

56 (1) Ensure that the instrument is switched off.

(2) Connect an 11 to 16 Volts DC supply to the DC power-input plug on the rear panel. The mating connector is a 2.1 mm coaxial socket.

CAUTION: SUPPLY POLARITY
THE POSITIVE SIDE OF THE SUPPLY MUST BE CONNECTED TO THE CENTER CONDUCTOR. EVEN THOUGH THE EXT. DC INPUT OF THE INSTRUMENT IS FUSE PROTECTED, IT IS STILL VITAL THAT THE EXTERNAL SUPPLY IS FUSED USING A 3 AMP SLOW-BLOW FUSE, SINCE THE INPUT IS NOT FLOATING.

(3) Set the INT/EXT switch on the rear panel to EXT.

(4) Switch the instrument on. Check that the instrument goes through the normal switch-on sequence.

57 If the external DC supply is interrupted the instrument will not necessarily power-up again when the supply voltage is restored. In this event, switch off and then on again using the front panel POWER switch.

Battery Charging

58 The battery is trickle-charged whenever the instrument is operated from an AC supply and the internal/external switch is at INTERNAL BATTERIES. To charge the battery at the full rate, connect the instrument to an external AC supply, switch on and select the standby mode.

SECTION 5 OPERATION VIA THE GPIB

INTRODUCTION

1 The instrument must be prepared for use in accordance with the instructions given in Section 3. If the instrument is being used for the first time, or at a new location, pay particular attention to the setting of the AC line voltage selector.

GPIB OPERATING MODES

2 The instrument can be operated via the GPIB in either the addressed mode or the talk-only mode.

TALK ONLY MODE

3 The talk-only mode may be used in systems which do not include a controller. Such a system permits remote reading of the instrument's measurement data, but the instrument is operated by means of the front panel controls as described in Section 4.

4 The rate at which measurements are made is determined by the instrument. The output buffer is updated at the end of each measurement cycle, overwriting the previous measurement data if this has not been transferred to the listener.

5 The transfer of data from the instrument to the listener is triggered by the listener. The instrument's output buffer is cleared when the data transfer is complete. Problems arising from the differences between the measurement rate and data transfer trigger rate are resolved according to the following protocol:

(1) If data transfer is in progress at the end of a measurement cycle, the updating of the output buffer is delayed. The data transferred will relate to the previous measurement cycle.

(2) If the data transfer trigger occurs during a measurement cycle and the output buffer is empty, data transfer will be delayed until the buffer is updated. the data transferred will then relate to the latest measurement cycle.

(3) If a measurement cycle is completed before the results of the previous cycle have been transferred to the listener, the buffer will be updated. The data for the previous cycle will be overwritten and lost.

6 The rate at which measurements are made can be controlled in the following ways:

(1) The gate time of the instrument (duration of the measurement cycle) can be controlled by choosing an appropriate display resolution.

(2) The instrument can be operated in the HOLD mode. Single measurement cycles can be triggered, when required, by means of the RESET/CONTINUE (Local) key.

(3) The display hold time can be set by entering a value, in seconds, into the sample store from the front panel.

7 The format of the data output is described in TABLE 5.1.

ADDRESSED MODE

8 In addressed mode operation, all the instruments functions, except power ON/OFF and the STANDBY/CHARGING facility, can be controlled by means of device-dependent commands, sent via the bus, when the instrument is addressed to listen.

9 The measurements made, and data regarding the instrument's status, can be read via the bus when the instrument is addressed to talk.

DATA OUTPUT FORMAT - NORMAL

10 The same output message format is used for the transmission of measured values and numbers recalled from the instrument's internal stores. The message consists of a string of 21 ASCII characters for each value transmitted. These are to be interpreted as shown in TABLE 5.1. The units should be assumed to be Hz, seconds, or a ratio, depending upon the commands previously given to the instrument.

DATA OUTPUT FORMAT - DUMP MODES

11 Dump mode output format is in the same output message format as normal data outputs. Display resolution is decreased thus decreasing computing and output time to allow for faster sample rates. Resolution of the readings is limited in the following ways:

(1) FREQ.C readings restricted to 10 kHz resolution.

(2) FREQ. A and FREQ. B readings restricted to four digits resolution.

12 Certain other modes are forced in Dump mode, see TABLE 5.11d. Refer to TABLE 5.3 and 5.4 for Dump mode byte functions.

TABLE 5.1

Output Message Format

Byte No	Interpretation	Permitted ASCII Characters
1	Function Letter	See TABLE 5.2
2	Function Letter	See TABLE 5.2
3	Space	Missing if SF81 is active
4	Sign of measurement	+ or -
5	Most Significant Digit	0 to 9 or .
6	Digit	0 to 9 or .
7	Digit	0 to 9 or .
8	Digit	0 to 9 or .
9	Digit	0 to 9 or .
10	Digit	0 to 9 or .
11	Digit	0 to 9 or .
12	Digit	0 to 9 or .
13	Digit	0 to 9 or .
14	Digit	0 to 9 or .
15	Digit	0 to 9 or .
16	Digit	0 to 9 or .
17	Least Significant Digit	0 to 9 or .
18	Exponent Indicator	E
19	Sign of exponent	+ or -
20	More Significant Digit	0 to 9
21	Least Significant Digit	0 to 9

NOTE 1:
Bytes 5 to 17 will always include 13 digits and a decimal point. Zeros will be added, where necessary, in the more significant digit positions.

NOTE 2:
The exponent indicated by bytes 20 and 21 will always be a multiple of three.

TABLE 5.2

Function Letters

Function	Function Letters
Frequency A	FA
Frequency B	FB
Frequency C	FC
Check	CK
Ratio C/B	CB
Ratio C/A	CA
Ratio B/A	BA
Recalled Data	**Function Letters**
Resolution	RS
Manual Store	MN
Offset Store	OS
Mult. Store	MU
Sample Rate Store	SA
Harmonic Number	HN
Local Oscillator Frequency	LO

NOTE: Bytes 1, 2 and 3 are not sent when special function 81 is active.

TABLE 5.3

Frequency C Dump

Byte	Character	Function
1	0 to 9	GHz × 10
2	0 to 9	GHz
3	0 to 9	MHz × 100
4	0 to 9	MHz × 10
5	0 to 9	MHz
6	0 to 9	kHz × 100
7	0 to 9	kHz × 10 Most significant digit

TABLE 5.4

Frequency A and B Dump

Byte	Character	Function
1	0 to 9	Most significant digit (see NOTE)
2	0 to 9	Digit
3	0 to 9	Digit
4	0 to 9	Digit
5	0 to 9	Least significant digit
6	0 to 9	Exponent
7	0 to 9	Exponent Value, most significant digit
8	0 to 9	Exponent value, least significant digit

NOTE:
Implied decimal point position is before Byte 1.

SERVICE REQUEST

13 The instrument can be set, by means of device-dependent commands, to generate the service request message (SRQ) when:

(1) A response message is ready.

(2) A 488.2 defined error occurs.

(3) A device defined error occurs.

(4) A change of frequency standard occurs.

(5) A user request for local control occurs.

14 The generation of the SRQ may also be inhibited. Generation of all SRQs is disabled when the instrument is first switched on.

STATUS BYTE

15 The format of the status byte, generated in response to a serial poll, is given in TABLE 5.6.

SETTING THE ENABLE REGISTERS

16 The Enable Registers to be set up are as follows:

(1) Service Request Enable Register - set using *SRE.

(2) Standard Event Status Enable Register - set using *ESE.

(3) Device Defined Event Status Enable Register - set using ESE.

17 Each bit in an enable register set to logic '1' enables the equivalent bit in its associated service register, see Table 5.5 for Associated Registers.

TABLE 5.5

Associated Registers

Enable Register	Service Register
Service Request Enable Register	Status Byte Register
Standard Event Status Enable Register	Standard Event Status Register
Device Defined Event Status Enable Register	Device Defined Event Status Register

18 The enable registers are set up by entering the register enable codes in NR1 format. NR1 format comprises decimal numbers in the range 0 to 255 representing the binary codes entered into the enable registers. See TABLE 5.6 to TABLE 5.8 for register contents.

19 The following example illustrates a register bit setting code and the NR1 format entry.

20 Example:

DIO Line Number: 8 7 6 5 4 3 2 1

Bit Number: 7 6 5 4 3 2 1 0

Required Bit Setting: 0 0 1 0 0 1 1 0

Binary Code: 100110

NR1 Format Decimal Number Code to be entered: 38

21 NR1 format codes can be entered as single digit numbers, two digit numbers or three digit numbers; e.g. 38, 038, 005, 05, 5, 120 etc.

TABLE 5.6

Status Byte and Service Request Enable Registers

DIO Line	Bit	Function
1	0	Not used - always logic 0
2	1	Not used - always logic 0
3	2	Not used - always logic 0
4	3	'1' = Summary of Device Event Status Register showing one or more logic 1s
5	4	'1' = Response message available
6	5	'1' = Summary of Standard Event Status Register showing one or more 1s
7	6	'1' = Service requested
8	7	Not used - always logic 0

TABLE 5.7

Standard Event Status and Enable Registers

DIO Line	Bit	Function
1	0	'1' = Operation Complete
2	1	Not used - always logic 0
3	2	'1' = Query Error (see NOTE 1)
4	3	Not used - always logic 0
5	4	'1' = Execution Error (see NOTE 2)
6	5	'1' = Command Error (see NOTE 3)
7	6	'1' = User Request (see NOTE 4)
8	7	'1' = Power On (after power interrupt)

NOTE 1:
Error generated either if controller tries to read the Output Queue when no output is available or data in the Output Queue is lost.

NOTE 2:
Error generated either if data associated with a particular command header is out of range, of the wrong type for a particular command, or if a valid program message could not be executed.

NOTE 3:
Command Error can be as a result of one of the following:

(1) Syntax error.

(2) Device has received an unrecognized or unimplemented header.

(3) 'GET' message has occurred within a program message.

(4) The command string will be correctly executed up to the point the error occurs. The remaining string up to the next command separator (;), or a valid program message terminator, will be ignored. Execution will continue as normal after reception of either of these delimiters.

NOTE 4:
Set to logic 1 when local control is requested by pressing the LOCAL key on the instrument front panel provided Local Lockout has not been sent.

TABLE 5.8

Device Defined Event Status and Enable Registers

DIO Line	Bit	Function
1	0	'1' = Indicates change of standard
2	1	Not used - always logic 0
3	2	Not used - always logic 0
4	3	'1' = Result out of range (see NOTE 1)
5	4	'1' = Internal counters overflow (see NOTE 2)
6	5	'1' = Local Oscillator out of lock (see NOTE 3)
7	6	'1' = Check mode error (see NOTE 4)
8	7	Not used - always logic 0

NOTE 1:
ER 02 on the display.

NOTE 2:
ER 03 on the display.

NOTE 3:
ER 04 on the display.

NOTE 4:
ER 50 on the display.

EXPLANATION OF RESPONSE TO INTERFACE MESSAGES

22 The instrument will respond to all valid device-dependent commands which are received after it has been addressed to listen. Device- dependent commands are recognized as such because they are transmitted with the attention (ATN) message false.

23 The instrument also responds to a number of multi-line interface messages. These are recognized because they are transmitted with the ATN message true. TABLE 5.9 gives the instrument's response to different bus messages. The following paragraphs detail the instrument's response to these messages. Any multi-line message not specifically mentioned is hand-shaken, but is otherwise ignored.

Address Messages

24 The instrument responds to address messages defined by the setting of the address switches, A1 to A5, on the rear panel. If these are set to 31 then the Address will default to 0.

25 On receipt of its listen address, the instrument becomes a listener. If it has been previously addressed to talk it ceases to act as a talker. If in the local control state when the address is received, the instrument goes to the remote control state provided that the REN message is true.

26 On receipt of its talk address, the instrument becomes a talker. If it has previously been addressed to listen it ceases to act as a listener. If in the local control state when the address is received, it will remain under local control.

27 If the instrument has been addressed to talk, and then receives the talk address of another device, it ceases to act as a talker.

Local Lockout

28 The instrument will respond to the local lockout (LLO) message regardless of its address state. The return-to-local function of the RESET/CONTINUE (Local) key on the front panel is disabled (the RESET/CONTINUE function remains enabled when in local control).

29 Local lockout is cleared by sending the remote enable (REN) message false. This returns all devices on the bus to the local control state.

Device Clear and Selected Device Clear

30 The instrument responds to the device clear (DCL) message and the selected device clear (SDC) message. It will only respond to the SDC message if it is a listener, but will respond to the DCL message regardless of its addressed state.

31 The instrument responds to either message by clearing any device dependent commands in its input buffer and any response message in the output queue.

TABLE 5.9

Response to Bus Messages

Message	Addressed State	Instrument Response
Address	Any	For listen address: Becomes a listener and goes to the remote control state. If previously addressed to talk, ceases to act as a talker. For talk address: Becomes a talker. If previously addressed to listen, ceases to be a listener. For talk address of another device: If previously addressed to talk, ceases to be a talker.
Local Lockout (LLO)	Any	LOCAL key disabled. (Cleared by sending the REN message false).
Device Clear (DCL)	Any	Clears any pending message in the Input Buffer and any response messages in the Output Queue.
Selected Device Clear (SDC)	Listen	As above.
Serial Poll Enable (SPE)	Any	Enters the serial poll mode state (SPMS). If addressed to talk while in this state, sends the status byte.
Serial Poll Disable (SPD)	Any	Enters the serial poll idle state (SPIS). If addressed to talk while in this state, sends data in the output message format.
Group Execute Trigger (GET)	Listen, and no measurement cycle in progress.	Triggers a measurement without command processing overhead and only after the Input Buffer is empty.
Go to Local (GTL)	Listen	Reverts to local control.
Untalk Unlisten	Talk Listen	Ceases to be a talker. Ceases to be a listener. The ADDR indicator turned off.

Serial Poll Enable and Serial Poll Disable

32 The instrument responds to the Serial Poll Enable (SPE) message and the Serial Poll Disable (SPD) message regardless of its addressed state.

33 The instrument responds to the SPE message by entering the serial poll mode state (SPMS). If the instrument is addressed to talk while in this state, it will put the status byte onto the bus instead of its normal data output string.

34 The instrument responds to the SPD message by leaving the SPMS and entering the serial poll idle state (SPIS). If the instrument is addressed to talk while in this state, it will put its data output string onto the bus provided data is available in the output buffer.

Group Execute Trigger

35 The instrument responds to the Group Execute Trigger (GET) message provided it is a listener and no measurement cycle is in progress. Except for the inability to retrigger during a measurement cycle, the response to the GET message is the same as to the common command *TRG.

Go to Local

36 The instrument responds to the Go to Local (GTL) message provided that it is a listener. The instrument reverts to the local control state, but remains addressed to listen. It return to remote control on receipt of the first byte of a device-dependent command.

Untalk and Unlisten

37 If addressed to talk, the instrument will go to the talker idle state (TIDS) on receipt of the untalk message. If addressed to listen, it will go to the listener idle status (LIDS) on receipt of the unlisten message. The ADDR indicator will be turned off.

INPUT COMMAND CODES

38 When the instrument is addressed it can be controlled by means of common commands given in Table 5.10 and device-dependent commands given in Table 5.11.

MESSAGE PROTOCOL AND SYNTAX

39 The IEEE 488.2 protocol provides a communication medium, using different types of messages, between a controller and controlled devices (i.e. Measuring instruments such as the Dana 2101 Microwave Counter). This medium is passed between controller and device via the GPIB Interface Bus.

40 The IEEE 488.2 Standard lays down hard and fast rules for message construction and content (referred to as PROTOCOL and SYNTAX).

System Message Traffic

41 Messages passed between controller and device consist of the following types:

(1) Program Messages - passed from controller to device. Program messages contain commands telling the device to do something, queries asking the device for data and status information, and data for setting device operating parameters. The device is defined as a LISTENER.

(2) Response Messages - Passed from device to controller. Response messages contain responses to queries and commands, data containing error information and results from measurements taken. The device is defined as a TALKER.

42 An example of the device as a listener is shown as follows:

Controller sends the command:	Device interprets and acts upon the command by selecting:
'FRQA'	'FRQA'

43 An example of the device as a talker is shown as follows:

Controller sends the query:	Device responds by sending the answer to the controller:
'GATE?'	'1' (indicating that the gate is open)

NOTE: In this example the device has first acted as a listener to enable it to receive the query, then acted as a talker to send the answer back to the controller as a response message.

Program Messages

44 Program messages are made up of Program Message Units (PMUs), PMU Separators (;) and a Program Message Terminator (PMT), see TABLE 5.12 Permitted Terminators. A program message is constructed as follows:

PMU ; PMU ; PMU ; PMU ; PMU PMT

45 Each PMU within the message is made up of a PMU Header (a mnemonic of ASCII characters), a Header separator (a white space character), Data and Data separators (,). A PMU is constructed as follows:

HEADER [ ] DATA , DATA , DATA , DATA ;

NOTE: In this example the white space character is represented by square brackets [ ]. Text spaces shown in the preceding and following examples are included for clarity only, no spaces in messages are to be used except where indicated by the square brackets.

46 This device accepts Program Messages into a buffer that can hold 10 string characters or 20 numerical characters.

Response Messages

47 Response messages are constructed in a similar manner to program messages. Response messages consist of Response Message Units (RMUs), RMU Separators (;) and a Response Message Terminator (RMT). The RMT is always the NL (or LF) character with EOI. A response message is constructed as follows:

RMU ; RMU ; RMU ; RMU ; RMU RMT

48 This device can store, in the Output Queue, five Response Message Units.

49 Each RMU within the message is made up of a RMU Header (a mnemonic of ASCII characters), a Header separator (a white space character), Response Data and Response Data separators (,). A RMU is constructed as follows:

HEADER [ ] RESPONSE DATA , RESPONSE DATA , RESPONSE DATA ;

NOTE: In this example the white space character is represented by square brackets [ ].

White Space Character

50 The white space character may be any ASCII encoded byte in the ranges of 0 to 9 and 11 to 32 inclusive. The most commonly used white space character is the space character (ASCII encoded byte 32) as generated by a QWERTY keyboard space bar.

OVERLAPPED/SEQUENTIAL COMMANDS

51 Every device-dependent command is defined as either sequential or overlapped.

52 A sequential command is started and completed before the succeeding command is executed.

53 An overlapped command is started but not necessarily completed before the succeeding command is started.

54 The synchronization commands (*WAI, *OPC, *OPC?) can be used to either control or indicate when the commands have been completed.

TABLE 5.10a

Common Commands

Code	Function	Explanation
*IDN?	Identification Query	Puts into the Output Queue a unique identification of the device. Response is divided into four fields separated by commas: Field 1 - Manufacturer Field 2 - Model number Field 3 - ASCII character 0 Field 4 - Software details NOTE: This Query should be the last Query message in any terminated message.
*RST	Reset	Sets device dependent functions to their power-up state.
*TST?	Self Test Query	Performs all tests not needing operator intervention. If all checks pass then ASCII 0 is placed in the Output Queue. If checks fail then the relevant number is placed in the Ouput Queue. The number output is in NR1 format.
*OPC	Operation Complete Command	Causes the instrument to generate the operation complete message in the Standard Event Status Register when all pending selected device operations are completed.
*OPC?	Operation Complete Query	As above, but places an ASCII 1 into the Output Queue instead of setting the operation complete message. NR1 format.
*WAI	Wait-to-continue Command	The instrument is prevented from executing any further commands or queries until there are not operations pending.

TABLE 5.10b

Common Commands (Continued)

Code	Function	Explanation
*CLS	Clear Status Command	Clears the Standard Event Register and the Device Event Register.
*ESE	Standard Event Status Enable Command	Sets the Standard Event Status Enable Register bits. Must be followed by decimal numeric data of NR1 format in the range 0 to 255. This regsiter determines which standard events will be reported to the Status Byte Register.
*ESE?	Standard Event Status Enable Query	Causes the instrument to put the current contents of the Standard Event Status Enable Register into the Output Queue. NR1 format.
*ESR?	Standard Event Status Register Query	Causes the instrument to put the current contents of the Standard Event Status Register into the Output Queue. This also clears the register. NR1 format.
*SRE	Service Request Enable Command	Sets the Service Request Enable Register bits. Must be followed by decimal numeric data of NR1 format in the range 0 to 255. When bits are set in this register, and provided that the corresponding summary bits in the Status Register are set, SRQ will be generated.
*SRE?	Service Request Enable Query	Causes the instrument to place the contents of the Service Request Enable Register into the Output Queue. NR1 format.
*STB?	Status Byte Query	Causes the instrument to place the contents of the status byte into the Output Queue. NR1 format. This returns the same value as a serial poll with the exception of bit 6 which is a summary of all other bits in the status byte.
*TRG	Trigger Command	Causes the instrument to trigger a measurement. Any existing measurement is aborted.

TABLE 5.11a

Device Dependent Commands

Code	Function	Explanation
Measurement Functions		
FRQA	Selects INPUT A	This command sent with required resolution. If resolution missing previous resolution used. Overlapped command (See NOTE 1).
FRQB	Selects INPUT B	This command sent with required resolution. If resolution missing previous resolution used. Overlapped command (See NOTE 1).
FRQC	Selects INPUT C	This command sent with required resolution. If resolution missing previous resolution used. Overlapped command (See NOTE 1).
CHECK	Selects 10 MHz check	This command sent with required resolution. If resolution missing previous resolution used. Overlapped command (See NOTE 1).
RABA	Selects Ratio of INPUT B to INPUT A	This command sent with required resolution. If resolution missing previous resolution used. Overlapped command (See NOTE 1).
RACA	Selects Ratio of INPUT C to INPUT A	This command sent with required resolution. If resolution missing previous resolution used. Overlapped command (See NOTE 1).
RACB	Selects Ratio of INPUT C to INPUT B	This command sent with required resolution. If resolution missing previous resolution used. Overlapped command (See NOTE 1).

TABLE 5.11b

Device Dependent Commands (Continued)

Code	Function	Explanation
Measurement Control		
HOLD	Selects HOLD Mode	The current reading is held in the display until another reading is triggered. Overlapped command (See NOTE 1).
MEAS?	New reading cycle	Causes the instrument to abandon the current reading, start a new reading cycle and place the calculated result into the Output Queue. Overlapped command (See NOTE 1).
MEAS:CONT?	Continuous stream of readings	Causes the instrument to take a continuous stream of radings and place them in the Output Queue. Each measurement is separated by ',' and no terminator is sent. When a new program message is sent this will generate a query error which cancels the MEAS:CONT? command. Overlapped command (See NOTE 2).
DISP?	Current displayed value placed in Output Queue	If this command is repeated without another measurement taking place or the display is reset, then a zero is placed in the Output Queue. DISP? is used with *TRG or GET with the instrument in HOLD Mode. If HOLD Mode is off the display is continuously updated and the results of *TRG or GET is lost. Sequential command.

TABLE 5.11c

Device Dependent Commands (Continued)

Code	Function	Explanation
Measurement Control (Continued)		
MAN	Controls Manual acquisition mode	This mode can be swtiched ON or OFF. Values can be stored in the MANUAL Store. One of these two parameters must be specified otherwise a command error is generated. If MAN ON is selected then TRACK ON or LOWFM ON commands are automatically disabled. When MAN OFF is selected then TRACK and LOWFM revert to their previous states. Allowed range 495 MHz - 26.505 GHz. Overlapped command (See NOTE 1).
LOWFM	Sets LOW FM to ON or OFF	This command switches the Low FM function ON or OFF in automatic acquisition mode. Selecting LOW FM when TRACK is ON disables TRACK function. Overlapped command (See NOTE 1).
TRACK	Sets TRACK to ON or OFF	This command switches the Track function ON or OFF in the acquisition mode. Selecting TRACK when LOWFM is ON disables LOWFM. Overlapped command (See NOTE 1).
OFFSET	Controls OFFSET function	Two parameters can be specified, first, the number to be stored, second, switching OFFSET to ON or OFF. If no parameters are specified then a command error is generated. Allowed range of the numerical input or displayed value is: $\pm 999.999999999 \times 10^{9}$ Overlapped command (See NOTE 1).

TABLE 5.11d

Device Dependent Commands (Continued)

Code	Function	Explanation
Measurement Control (Continued)		
MULT	Control Multiplier function	Two parameters can be specified, first, the number to be stored, second, switching MULT to ON or OFF. If no parameters are specified then a command error is generated. Allowed range of the numerical input or displayed value is: ±999.999999999 × 109. Overlapped command (See NOTE 1).
SAMPLE	Controls display sample rate	This function enables the read rate to be varied by specifiying a display hold time. The allowed range is 0 to 10 seconds, numbers are rounded to the nearest 10mS. Sequential command.
DUMP	Controls Dump mode	The following modes are forced when DUMP Mode is enabled: FREQ C - selected if any ratio or check is selected, 10 kHz resolution. When DUMP Mode is disabled the selected function will be enabled. FREQ A & B - 4 digits resolution. MULT - OFF. OFFSET - OFF. ALL SPECIAL FUNCTIONS - disabled except 11, 41, 42, 43, 61 (VXI only), and 71. DUMP MODE CONDITIONS: When activated display is blanked and not further update occurs until DUMP is disabled. MEAS:CONT? - used to start a stream of continuous readings at maximum speed. MEAS?, *TRG and GET commands may be used with DUMP, but returns only one measurement result. Overlapped command (See NOTE 1).

TABLE 5.11e

Device Dependent Commands (Continued)

Code	Function	Explanation
Query Commands		
MAN?	Manual store contents query	Places the contents of the Manual Store in the Output Queue. NR3 format. Sequential command.
OFFSET?	Offset store contents query	Places the contents of the Offset Store in the Output Queue. NR3 format. Sequential command.
MULT?	Multiplier store contents query	Places the contents of the Multiplier Store in the Output Queue. NR3 format. Sequential command.
SF?	Special Function query	Places the Special Functions status in the Output Queue. Sequential command.
SAMPLE?	Sample store contents query	Places the contents of the Sample Store in the Output Queue. NR1 format. Sequential command.
STD?	Standard in use query	Puts a numerical value in the Output Queue according to the standard in use: '1' = Internal standard '0' = External standard. NR1 format. Sequential command.
ESR?	Device Event Register query	Places the contents of the Device Event Register into the Output Queue, the register is then cleared. NR1 format. Sequential command.

TABLE 5.11f

Device Dependent Commands (Continued)

Code	Function	Explanation
Query Commands (Continued)		
ESE?	Device Event Status Enable Register query	Places the contents of the Device Event Status Enable Register into the Output Queue. NR1 format. Sequential command.
GATE?	Gating status query	Places a numerical value in the Output Queue according to the status of the gate signal: '0' = Gate closed '1' = Gate open. NR1 format. Sequential command.
LO?	Local Oscillator store query	Places the contents of the Local Oscillator store into the Output Queue. NR1 format. Sequential command.
HN?	Harmonic Number store query	Places the contents of the Harmonic Number store into the Output Queue. NR1 format. Sequential command.
General Commands		
FP	Front Panel display control	When OFF is selected the display is blanked. This command is only disabled by using the command with ON parameter or switching the instrument off then on again. Sequential command.
LO	Local Oscillator setting	Sets the value of the Local Oscillator when SF41 is active. Allowed range of the numerical or displayed value is 294.0 MHz to 354.0 MHz. Numbers are rounded to the nearest 0.1 MHz. Sequential command.

TABLE 5.11g

Device Dependent Commands (Continued)

Code	Function	Explanation
General Commands (Continued)		
HN	Harmonic Number setting	Sets the value of the Harmonic Number when SF41 is active. Allowed range of the numerical or displayed value is ±-2 to ±90. Numbers are rounded to the nearest integer. Sequential command.
ESE	Device Defined Event Status Enable Command	Sets the Device Defined Event Status Enable Register. Allowed range of numbers is 0 to 255. NR1 format. Sequential command.
SF	Controls Special Functions	'OFF' turns the Special Functions off but preserves those selected. 'ON' switches on those Special Functions. Overlapped command (See NOTE 1).

NOTE 1:
These overlapped commands are defined as complete when the gate control circuit is armed, or if FREQ C is in use, the acquisition cycle has commenced.

NOTE 2:
This overlapped command is defined as complete when the result is placed into the Output Queue. If the compound command CONT is used, the command is still complete at the same time but only at the first result received. If MULT MEAS? is used in the same string then the operation complete flag will be set when the first MEAS? is complete.

TABLE 5.12

Permitted Terminators

1	2	3
LF	LF EOI true	Last Character EOI true

NOTE:
LF = Line Feed
EOI = END or IDENTITY

TABLE 5.13

Numerical Input Format

Byte No	Interpretation	Permitted ASCII Characters
1	Sign of Mantissa	+ or -
2	Most Significant Digit	0 to 9 or .
3	Digit	0 to 9 or .
4	Digit	0 to 9 or.
5	Digit	0 to 9 or .
6	Digit	0 to 9 or .
7	Digit	0 to 9 or .
8	Digit	0 to 9 or .
9	Digit	0 to 9 or .
10	Digit	0 to 9 or .
11	Digit	0 to 9 or .
12	Digit	0 to 9 or .
13	Digit	0 to 9 or .
14	Least Significant Digit	0 to 9 or .
15	Character has no meaning	White Space
16	Exponent Indicator	E
17	Character has no meaning	White Space
18	Sign of Exponent	+ or -
19	More Significant Digit	0 to 9
20	Digit	0 to 9
21	Digit	0 to 9
22	Digit	0 to 9
23	Least Significant Digit	0 to 9

NOTE 1:
At least one exponent digit must be used if 'E' (bit 16) is present.

NOTE 2:
The numerical input format conforms to IEEE 488.2 and is based on NR1, NR2 and NR3 formats. Any number input that deviates from these formats will generate a command error. If the number is out of range for a particular command header, then an execution error is reported. For some commands the resolution of the mantissa is limited.

TABLE 5.14

Gate Times for FREQUENCIES A and B

Number of digits in FREQ A, FREQ B & CHECK	Gate Time	Resolution Number
10	20 s	10
9	1 s	9
8	100 ms	8
7	10 ms	7
6	1 ms	6
5	1 ms	5
4	1 ms	4
3	1 ms	3

TABLE 5.15

Gate Times for FREQUENCY C

Frequency GHz	Resolution			
	1 Hz	10 Hz	100 Hz	1 kHz
0.5 - 1.0	100 ms	10 ms	1 ms	1 ms
1.0 - 4.0	200 ms	20 ms	2 ms	1 ms
4.0 - 8.0	400 ms	40 ms	4 ms	1 ms
8.0 - 12.0	600 ms	60 ms	6 ms	1 ms
12.0 - 16.0	800 ms	80 ms	8 ms	1 ms
16.0 - 20.0	1 s	100 ms	10 ms	1 ms

TABLE 5.16

Special Function Codes

Function	Code
Deselects Channel A filter	10
Selects Channel A filter	11
Cancels Smooth function	20
Selects Smooth function (See NOTE 1)	21
Cancels all group 30 special functions	30
Displays Local Oscillator Value (See NOTE 2)	31
Displays Intermediate Frequency (See NOTE 3)	32
Displays Harmonic Number as an integer (See NOTE 3)	33
Displays Harmonic Number with fractional part (See NOTE 3)	34
Displays IF Detector Status (See NOTEs 3 & 4)	35
Displays LP Filter Status (See NOTEs 3 & 4)	36
Displays LO Lock Line Status (See NOTE 7)	37
Cancels all group 40 special functions	40
Allows setting of LO & Harmonic Number (See NOTEs 3 & 5)	41
Switches LO Off under all conditions (Quiet Mode)	42
Disables IF output under all conditions	43
Cancels all group 50 special functions	50
Ignore IF level detector	51
Cancels all group 70 special functions	70
Initiates front panel display checks	71
These codes are reserved for diagnostic purposes and are described in the Maintenance Manual (See NOTE 6)	72 73 74 75
Leading (function) letters in O/P string	80
No leading (function) letters in O/P string	81
Cancels group 90 special functions	90
Enables hardware ratio B/A	91

NOTE 1: This function does not operate on diagnostic special functions.

NOTE 2: This function only operates during INPUT C measurements and displays the Local Oscillator selected to make a measurement.

NOTE 3: Operates under same conditions as Special Function 31.

NOTE 4: '0' displayed = Detector False.
'1' displayed = Detector True.
(Special Function 41 must also be active).

NOTE 5: MANUAL LED is on, LO and Harmonic Number (HN) store both active. To access LO use TRACK key, to access HN use LOWFM key.

NOTE 6: Special Functions 71 to 75 can be entered into the special functions register at any time. They are active only when the instrument is in Check Mode.

NOTE 7: '0' displayed = In lock, '1' displayed = Out of Lock.

TABLE 5.17

Special Function Request (SF?) Response Format

SF Groups >	10 20 30 40 50 60 70 80 90
Response Format >	n , n , n , n , n , n , n , n , n

TABLE 5.18

Alphabetic List of Required Command Codes

Code	Function	Code	Function
*CLS	Clear status	*OPC?	Operation Complete Query
*ESE	Standard Event Status Event	*RST	Reset
		*SRE	Service Request Enable
*ESE?	Standard Event Status Event Query	*SRE?	Service Request Enable Query
*ESR?	Standard Event Status Query	*STB	Status Byte Query
		*TST	Self Test Query
*IDN?	Identification Query	*WAI	Wait to Continue
*OPC	Operation Complete		

TABLE 5.19

Alphabetic List of Optional Command Codes

	Code	Function	Code	Function	
o	CHECK	Selects 10MHz check	LOWFM	Controls Low FM	o
s	DISP?	Displays value in output queue	MAN	Controls manual select	o
			MAN?	Manual store query	o
o	DUMP	Control DUMP mode	MEAS?	New reading cycle	o
s	ESE	Device Event Status Enable	MEAS: CONT?	Continuous stream of readings	o
s	ESE?	Device Event Status Register query	MULT	Controls Multiplier	o
			MULT?	MULT store query	s
s	ESR?	Device Event Register query	OFFSET	Controls Offset	o
			OFFSET?	Offset store query	s
s	FP	Front panel display control	RABA	Selects RATIO B/A	o
			RACA	Selects RATIO C/A	o
o	FREQA	Selects INPUT A	RACB	Selects RATIO C/B	o
o	FREQB	Selects INPUT B	SAMPLE	Controls display sample rate	s
o	GREQC	Selects INPUT C			
s	GATE?	Gating status query	SAMPLE?	Sample store query	s
s	HN	Harmonic number setting	SF	Controls Special Functions	o
s	HN?	Harmonic number store query	SF?	SF query	s
o	HOLD	Selects HOLD mode	STD?	Standard in-use query	s
s	LO	Local oscillator setting			
s	LO?	Local oscillator store query	TRACK	Controls Track	o
			*TRG	Trigger command	

NOTE:
o denotes an overlapped command.
s denotes a sequential command.

SECTION 6 PRINCIPLES OF OPERATION

INTRODUCTION

1 This section describes the principles of operation of the instrument, with respect to a number of block diagrams in the text, and describes the significant features of the circuits used with respect to the circuit diagrams given in Section 8. The block diagrams are annotated with the main circuit references to simplify cross referencing between the block diagram and circuit diagram.

2 In the circuit descriptions the integrated circuits are referred to by the circuit reference given on the appropriate circuit diagram. Note that a separate series of numbers, starting at IC1, is allocated to each assembly. Where an integrated circuit package contains more than one circuit, suffix letters are used to distinguish between them. Where it is required to identify a particular pin of an integrated circuit, the circuit reference, with suffix letter if appropriate, is followed by an oblique stroke and the required pin number.

FUNCTIONAL SYSTEMS

3 The instrument contains a number of functional systems, these are:

(1) The Channel A System.

(2) The Channel B System.

(3) The Channel C System.

(4) The Measurement System.

(5) The Display System.

(6) The Keyboard System.

(7) The Microprocessor System.

(8) The Standby and IRQ System.

(9) The Power Supply System.

(10) The Internal Frequency Standard System.

4 The functional relationship between the systems is illustrated in Fig. 6.1. The measurement system is internally configured by the microprocessor system according to the instructions entered via the keyboard or GPIB system. The signal to be measured and the signal from the frequency standard are fed to the measurement system. The measured result is passed to the microprocessor system. If mathematical manipulation of the result is required, this is performed by the microprocessor before the final output is passed to the display or GPIB system.

5 The standby and IRQ system handles instructions to switch to standby, received from the keyboard system or the battery pack option (if fitted).

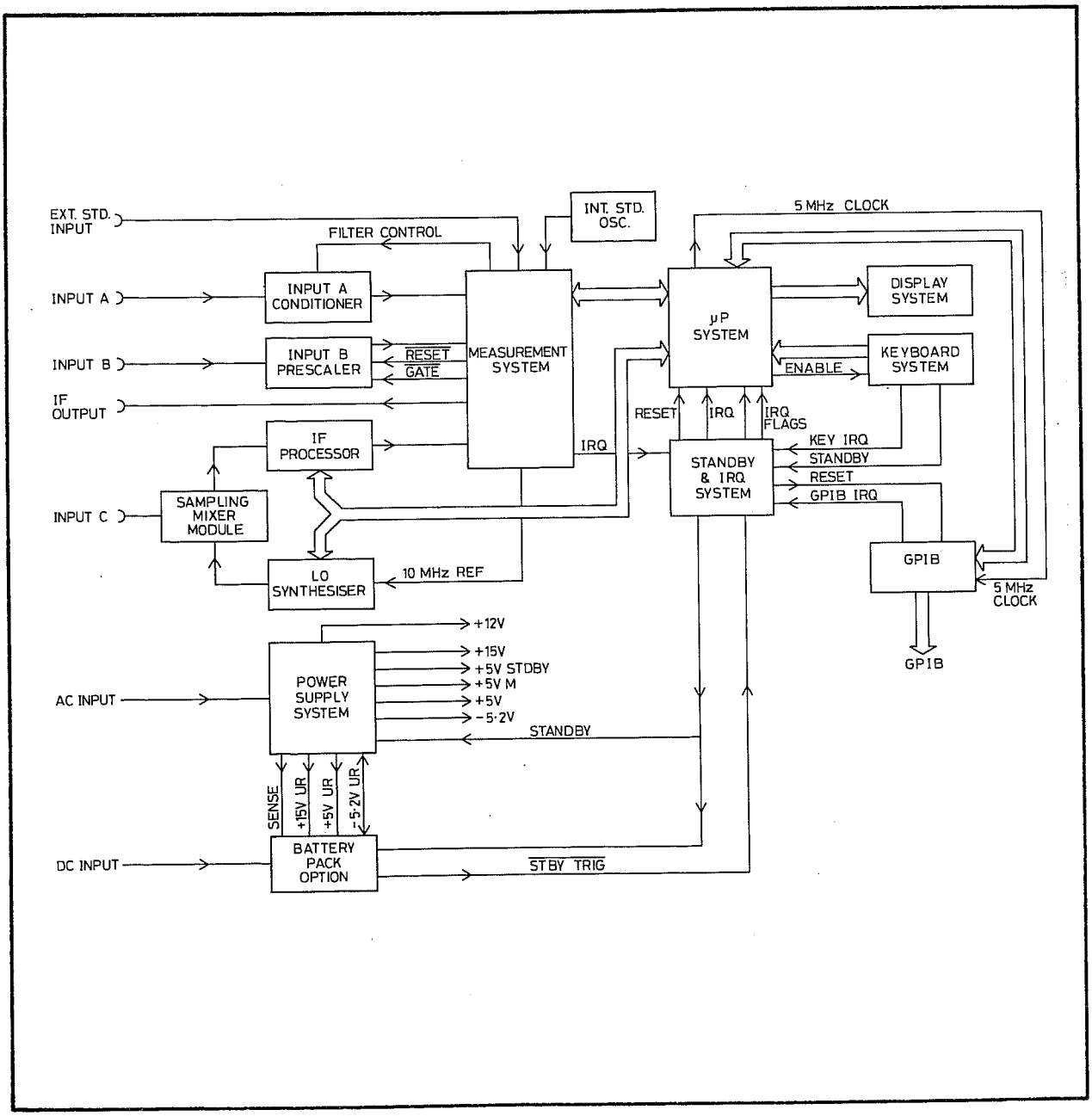


Fig. 6.1 Functional Block Diagram

THE CHANNEL A SYSTEM

Functional Description

6 The channel A system processes the signals applied at INPUT A to produce a pair of differential signals that are fed to the measurement system. A block diagram is given in Fig. 6.2.

7 INPUT A covers the frequency range of 10 Hz to 80 MHz and is an AC coupled 1 MegOhm/35 pF input. An input protection signal clamp feeds a FET buffer stage. The output of the buffer is fed via a selectable 50 kHz low-pass filter to a Schmitt-trigger comparator. The differential outputs of the comparator feed the measurement system. The 50 kHz filter, when selected, reduces the effects of high frequency noise on low frequency measurements.

Circuit Description

8 The circuit diagram is shown in Fig. 5. The signal at INPUT A is coupled via SK5 to DC blocking capacitor C1. R2 acts as the input termination. The signal clamp, comprising R1, D1, D2, D6, R3, R158, C2 and C98, limits the signals applied to the following buffer amplifier. The buffer amplifier comprises Q1, Q2 and R4 to R6. The base emitter voltage of Q2 imposed on R4 stabilizes the operating current of Q1.

9 C3, C4 and C5 provide broadband AC coupling. With RL1b de-energized, the signal is routed via potential divider R20, R10 and the comparator IC25a. When the low-pass filter is selected, RL1b is energized and the filter comprising R20, L1, R10, C38 and C39 is inserted into the signal path.

10 The other input of IC25a is set to 0 V reference. Hysteresis control for the comparator is provided by R7, via R8, R9 and C6. The comparator's differential outputs are fed to the measurement system via two 50 Ohms microstrip lines.

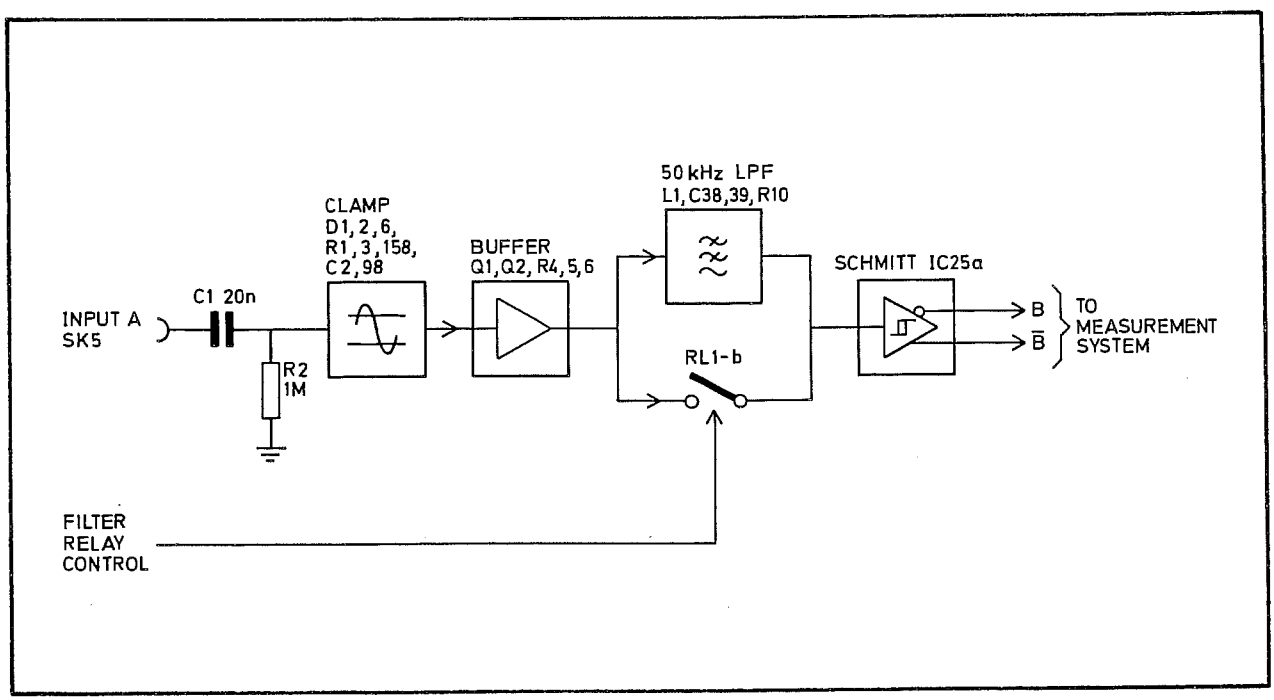


Fig. 6.2 The Channel A System

THE CHANNEL B SYSTEM

Functional Description

11 The channel B system processes the signals applied at INPUT B and feeds it to the measurement system. A block diagram is given in Fig. 6.3.

12 The input is protected by a fuse, mounted in the input connector, and by a signal limiting circuit. This is followed by an automatic level control circuit, which reduces the range of signal level applied to the amplifier.

13 After amplification the signal is prescaled by 64 before being passed via a buffer and a signal gate to the measurement system.

14 The amplitude of the signal at the amplifier output is monitored by a detector and comparator. The comparator output controls the low-signal latch. If the detector output is below the threshold, the latch is set and the output to the measurement system is inhibited by the signal gate. When the detector output goes above the threshold the low-signal latch is armed, and opens the signal gate on the next signal edge from the prescaler. This enables the instrument to make measurements on bursts of signal.

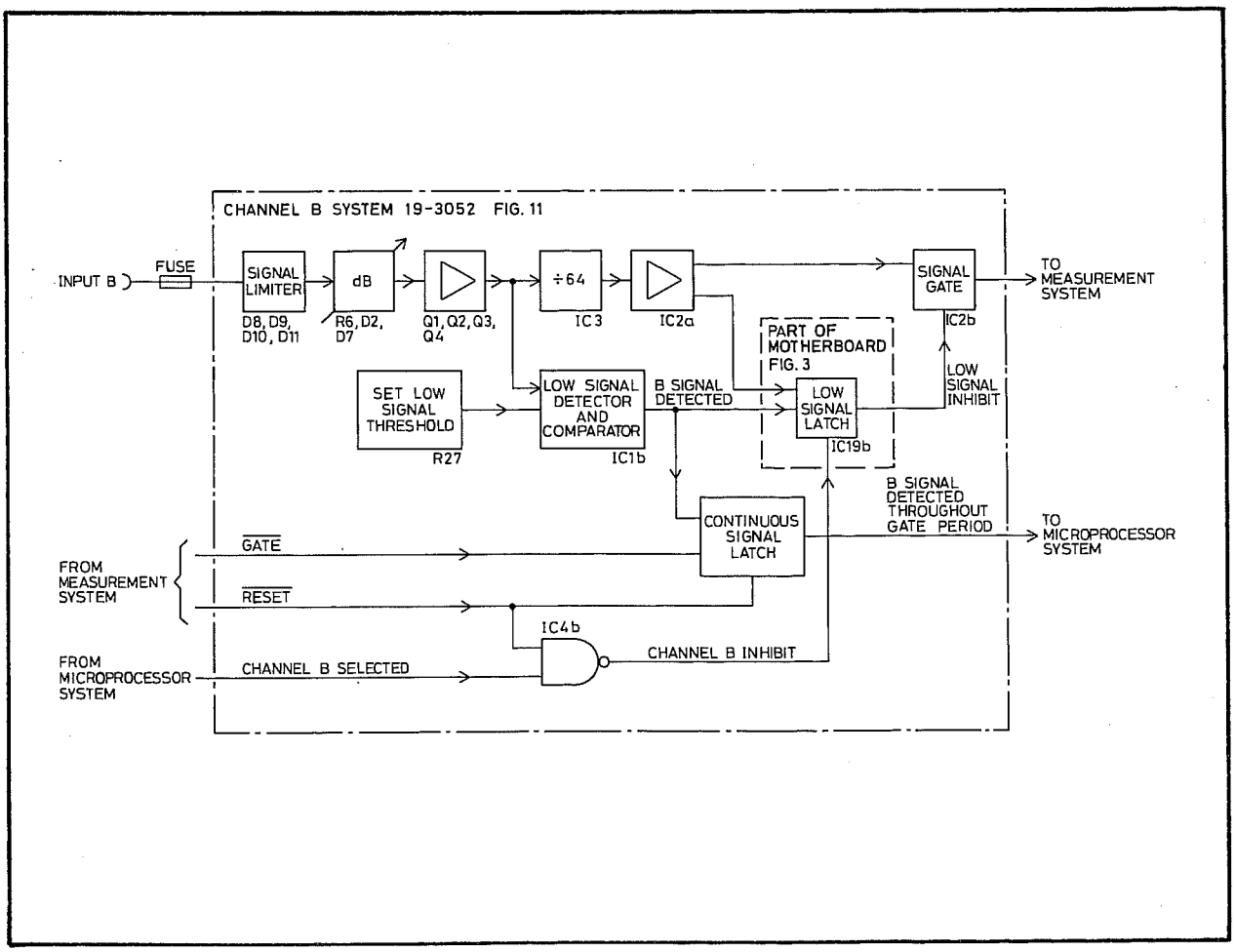


Fig. 6.3 The Channel B System

15 The detector output is also applied to the continuous signal latch. This latch is reset at the beginning of each gate period, and is set if the detector output falls below the threshold level. The microprocessor checks the latch status at the end of the gate period. If the measured signal falls below the threshold level during this period, the measured result is set to zero.

16 If channel B is not selected, the low-signal latch is held reset by a control signal from the microprocessor system and the output to the measurement signal is inhibited.

Circuit Description

17 The circuit diagram is shown in Fig. 12 in Section 8. The signal to be measured is connected via A1 (INPUT B). The circuit is protected by the fuse, which is mounted within A1. The signal amplitude is limited by the diode clamp comprising D8, D9, D10 and D11.

18 A measure of automatic gain control is achieved by means of an attenuator, formed by R6 and the impedance of the PIN diodes, D2 and D7. The detector comprising D1, D3, R7 and C48, produces a negative voltage proportional to the signal amplitude. A direct current proportional to this voltage flows through the PIN diodes via L1. The impedance of the diodes decreases if the current increases, so that changes in signal amplitude are offset by changes in attenuation.

19 The signal passes through four amplifier stages, incorporating Q1, Q2, Q3 and Q4. The amplified signal is fed to the counter, IC3, via the shaping circuit formed by R37, C46 and R36.

20 The signal frequency is prescaled by 64 in IC3 and buffered in IC2a. Provided that channel B is selected and the amplitude of the signal is adequate, the output at IC2a/2 passes to the measurement system via the gate, IC2b, and SK7 pin 5.

21 The signal at the output of Q4 is fed to the low-signal detector, D5 and C23. The comparator, IC1b, compares the detector output with a threshold voltage, set by R27. The comparator output is at logic '1' if the detector output is below the threshold (signal amplitude too low for accurate counting).

22 The logic level at the comparator output is inverted in IC1a to become the 'DET' signal. This is fed via SK7/14 to the 'D' input of the output synchronizer, IC9b on the 19-3022 motherboard assembly. The 'B/64' output of IC2a at SK7/8 is fed to the clock input of IC9b. If there is insufficient signal amplitude, 'DET', and hence the 'D' input of IC9b, will be at logic '0' and this causes the output at IC9b/14 to be at a permanent logic '1'. Since this output is WIRE ORed to IC2a/2, via SK7/7, it will force IC2a/2 to also be at a permanent logic '1'. In this way the 'B O/P' from IC2b is inhibited. When an input signal of sufficient amplitude is applied, 'DET', and hence the 'D' input of IC9b, will be at logic '1'. This is transferred as a logic '0' to the NOT Q output of IC9b synchronizer with the next rising edge on the 'B/64' line. This removes the clamp from the NOT 'C/64' line and allows the 'B O/P' from IC2b to toggle. In this way 'B O/P' only ever carries whole prescaler output pulses.

23 The NOT GATE signal enters the system at SK7 pin 17 and is inverted in IC1c. The resulting signal and the output of the comparator, IC1b, are fed to IC4a. If both inputs are at logic '1', indicating that the channel B signal level is too low while the gate is open, the continuous signal latch, IC4c and d, is set. The latch output is fed to the microprocessor system via SK7 pin 11, and prevents the result of any measurement made during that gate period from being displayed.

24 When INPUT B is not selected, SK7 pin 16 is at logic '0'. This is inverted and buffered in IC4b and IC1d and is fed to IC9b (on the motherboard) via SK7 pin 13. IC9b is held reset, thus inhibiting IC2b, via SK7 pin 7, and hence inhibiting the 'B O/P'.

THE CHANNEL C SYSTEM

Functional Description

25 Signals in the frequency range of 500 MHz to 20 GHz are applied at INPUT C. They are mixed via a sampling mixer, down to an intermediate frequency (IF) which is low enough to be acquired and counted by the measurement circuits. The process of mixing down used in the 2101 is known as harmonic heterodyning and is described under the title 'Harmonic Heterodyning'. The process of acquiring a signal is described in the section following 'Harmonic Heterodyning'. A functional block diagram is given in Fig. 6.4.

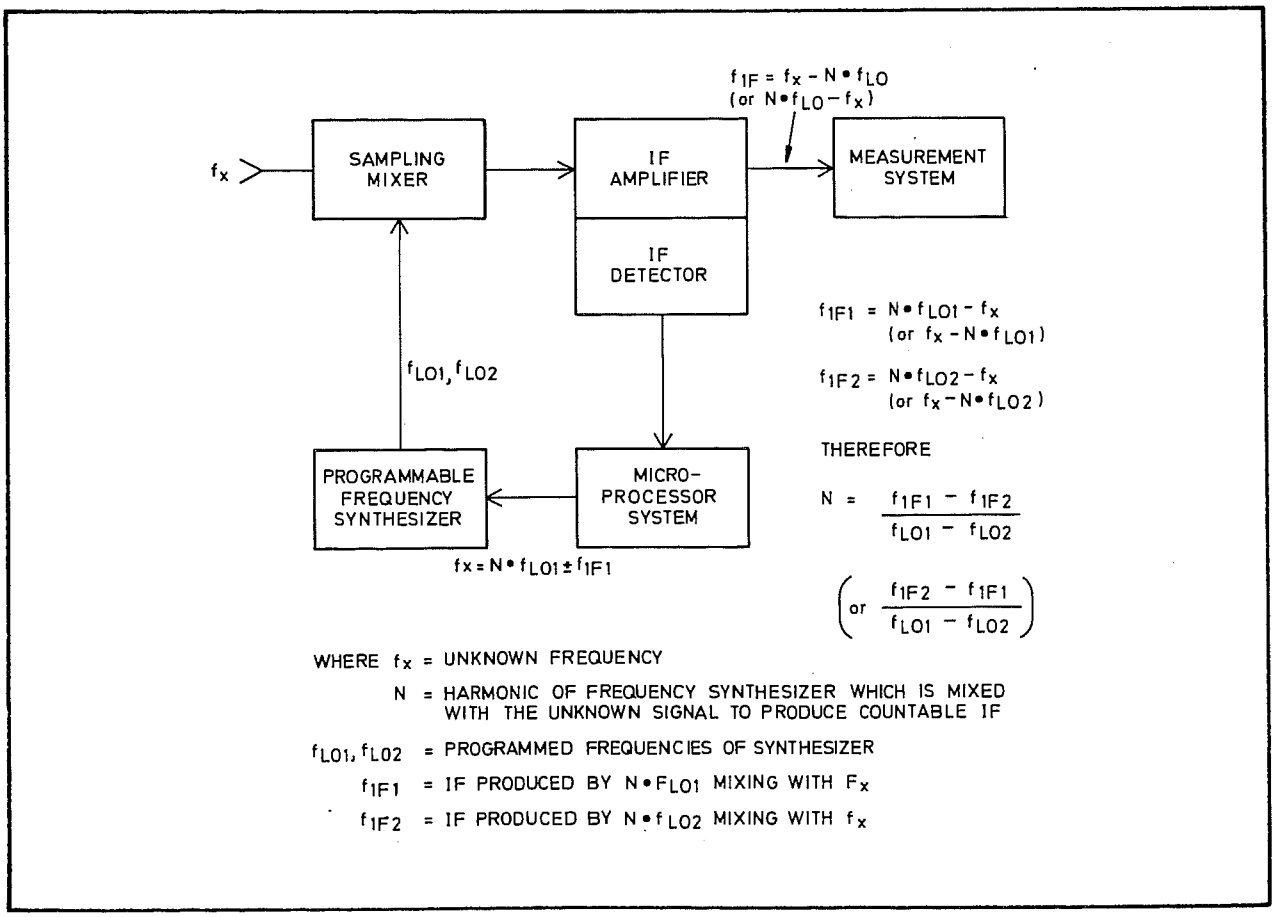


Fig. 6.4 The Channel C System

Harmonic Heterodyning

26 Basic heterodyning is the process in which an unknown signal, fX, is mixed with a local oscillator (LO) frequency to produce an intermediate frequency (IF). Harmonic heterodyning is an extension of the process in which the input signal is mixed with one or more harmonics of a local oscillator signal to produce at least one IF. The relationship is as follows:

$$fIF = N.fLO - fX \quad (\text{for } fX < N.fLO)$$

OR

$$fIF = fX - N.fLO \quad (\text{for } fX > N.fLO)$$

Where 'N' is the local oscillator harmonic number.

Acquiring a Signal Using Harmonic Heterodyning

27 The programmable LO frequency synthesizer is stepped from its highest frequency downwards until the IF detector signals to the microprocessor that an IF lies within the range of the counting circuits, both in terms of level and frequency. At this point the LO sweep is stopped, and the counter measures fIF. fLO is accurately known since it is from a synthesized source locked to the counter's timebase, and hence the counter must determine the actual harmonic in use, N, and the sign of the mix, in order to compute fX, the unknown frequency.

28 To do this, the LO is stepped a known amount and the IF re-measured. The amount that the IF moves yields the harmonic number, and the direction of movement relative to the direction of LO movement yields the sign of the mix. This is shown mathematically as follows:

NOTE: This description only holds true for signals carrying little or no frequency modulation (FM), see 'Tolerance to FM' following this description.

for $N.fLO > fX$:

$fIF1 = N.fLO1 - fX$ and $fIF2 = N.fLO2 - fX$

$$\text{hence } N = \frac{fIF1 - fIF2}{fLO1 - fLO2} \text{ rounded to the nearest integer.}$$

and for $N.fLO < fX$:

$fIF1 = fX - N.fLO1$ and $fIF2 = fX - N.fLO2$

$$\text{hence } N = \frac{fIF2 - fIF1}{fLO2 - fLO1} \text{ rounded to the nearest integer.}$$

To calculate N, the formula $N = \frac{fIF1 - fIF2}{fLO1 - fLO2}$ is used.

Then fX is computed as follows:

fX = N.fLO1 - fIF1, assuming that fIF2 > fIF1,

fX = N.fLO1 + fIF1, assuming that fIF2 < fIF1.

29 The measurement accuracy is limited only to the residual stability of the LO and the counter's timebase accuracy.

Tolerance to FM

30 Many RF and Microwave signals carry significant amounts of FM. The 2101 has in-built features that help it to cope with signals of this nature. To do this, the correct computation of 'N', the harmonic number, has to be maintained in the presence of FM. The following technique is used, and reference should be made to Fig. 6.5.

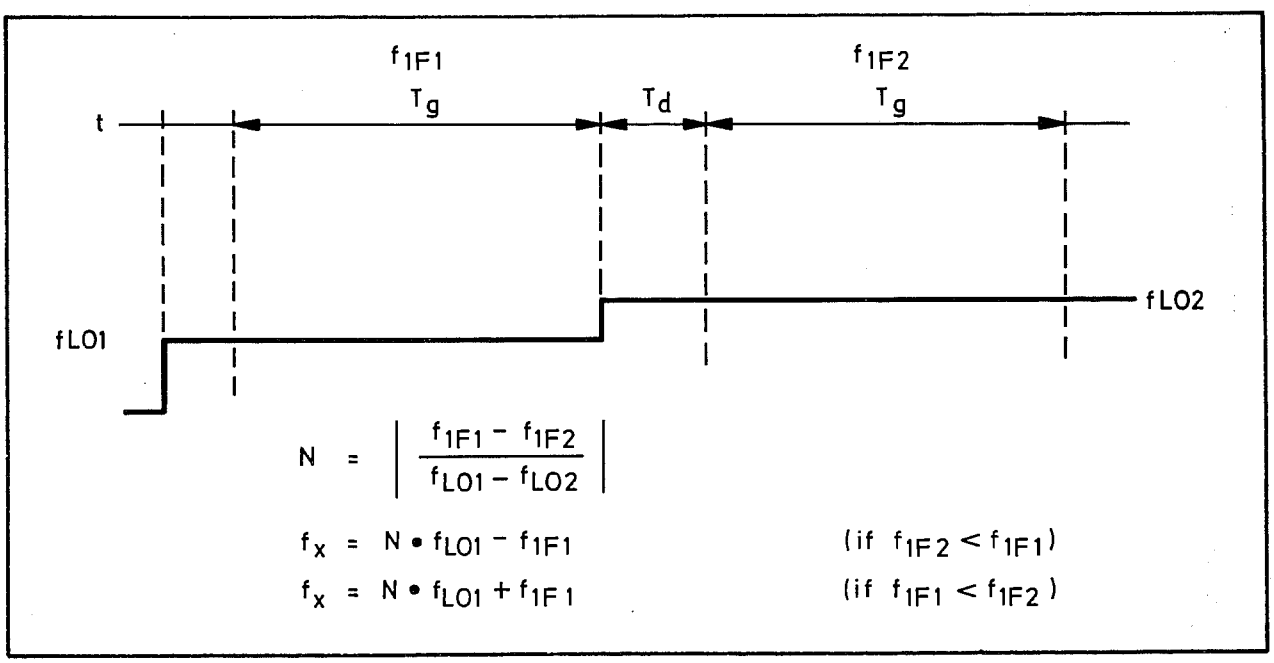


Fig. 6.5 Normal Acquisition Timing Diagram

31 The LO is swept down from its highest value. As soon as the IF detector detects a countable signal, the LO sweep is stopped and a 'dead time' (Td) starts. Td allows the LO to stabilize in frequency. At the end of Td, the gate time (Tg) begins, during which fIF1 is measured.

32 The LO is offset again and a second Td allows the LO to stabilize at the new frequency. At the end of Td, the second Tg begins and a second reading is taken, fIF2.

33 When calculating 'N', the microprocessor rounds the answer to the nearest integer. If the error due to FM is <0.5 then the answer is rounded down, and the integer value of 'N' remains unaltered.

34 Both Td and Tg affect the FM tolerance and are chosen so that a maximum peak deviation of 10 MHz and FM rates down to 1 kHz can be tolerated. If LOW FM mode is used, FM rates down to 45 Hz can be tolerated.

Amplitude Discrimination

35 The instrument can discriminate against unwanted signals that are sufficiently below the level of the wanted signal. If the wanted signal, in the range 500 MHz to 20 GHz, is 20 dB greater in amplitude than any unwanted signal then the instrument always acquires and counts the wanted signal. However, the instrument is able to discriminate against unwanted signals that are within 500 MHz and are only 6 dB lower in amplitude than the wanted signal. This is possible due to two characteristics of the IF amplifier:

(1) The IF bandwidth.

(2) IF amplifier limiting.

36 The IF bandwidth is set at half the maximum LO frequency, which ensures that any input signal will be mixed down and appear within the IF bandwidth. The IF band contains IFs from every input signal within the range 500 MHz to 20 GHz.

To achieve this complete coverage, the following must be true:

$$N.fLO + fIF' = (N + 1).fLO - fIF'$$

where fIF' is the cut-off frequency of the IF amplifier.

Therefore:

$$fIF' = \frac{fLO}{2}$$

This has a maximum value $fIF'\ max = \frac{fLO\ max}{2}$, which sets the design limit for the upper cut-off frequency of the IF amplifier.

37 The IF amplifier limits all IFs produced by signals greater than or equal to the instruments sensitivity level. This ensures that the dominant signal is always counted. The presence of subordinate signals causes phase modulation of the limited dominant signal but this is small enough not to introduce errors into the IF count.

Sensitivity

38 Two major factors affect the sensitivity performance. One is the conversion efficiency of the sampler, this determines the minimum IF level that must be handled by the IF system. The second is the effective noise bandwidth of the IF system, and hence affects the overall signal to noise ratio (SNR). Careful control of IF design bandwidth and roll off is required to maximize the SNR of the system.

Sampling Mixer Module

39 The sampling mixer converts microwave input signals in the range 500 MHz to 20 GHz to a band of IFs low enough in frequency to be handled by the measurement circuits. The local oscillator (LO) module supplies a relatively high signal to the sampling mixer, in the range 292.5 MHz to 354.5 MHz.

40 The sampling mixer contains an impulse generator which is driven from the LO signal and which generates very narrow pulses (of the order of 30 ps) at the local oscillator rate. These pulses are used to turn on a sampling gate within the mixer. This gate samples the instantaneous amplitude of the RF signal and holds this amplitude, with some loss, until the next sampling pulse occurs. This action causes a low frequency version of the input signal (IF) to be built up gradually over many cycles of the input.

41 The narrow pulses generated by the impulse generator in the sampling mixer have a spectrum which consists of harmonics of the LO signal stretching to 20 GHz and beyond. Any input signal within the instruments bandwidth will mix with these harmonics to produce a range of IFs, one of which will be within the IF bandwidth of the subsequent circuits.

42 The output of the sampling mixer is fed to the IF processor. This has a flat frequency response, symmetrical limiting and LO filtering.

THE LO FREQUENCY SYNTHESIZER

Functional Description

43 The Lo frequency synthesizer generates a signal in the range 292.5 MHz to 354.5 MHz, in 100 kHz steps. This signal is used to drive the LO input of the sampling mixer. The frequency is programmable via the microprocessor bus. A block diagram is given in Fig. 6.6.

44 The output of the voltage controlled oscillator (VCO) is divided down, and the phase of the resulting signal is compared with that of a reference signal. The comparison takes place in a phase sensitive detector (PSD) whose output is an error voltage proportional to the phase difference between the two signals. This error voltage pulls the VCO into lock with the reference signal.

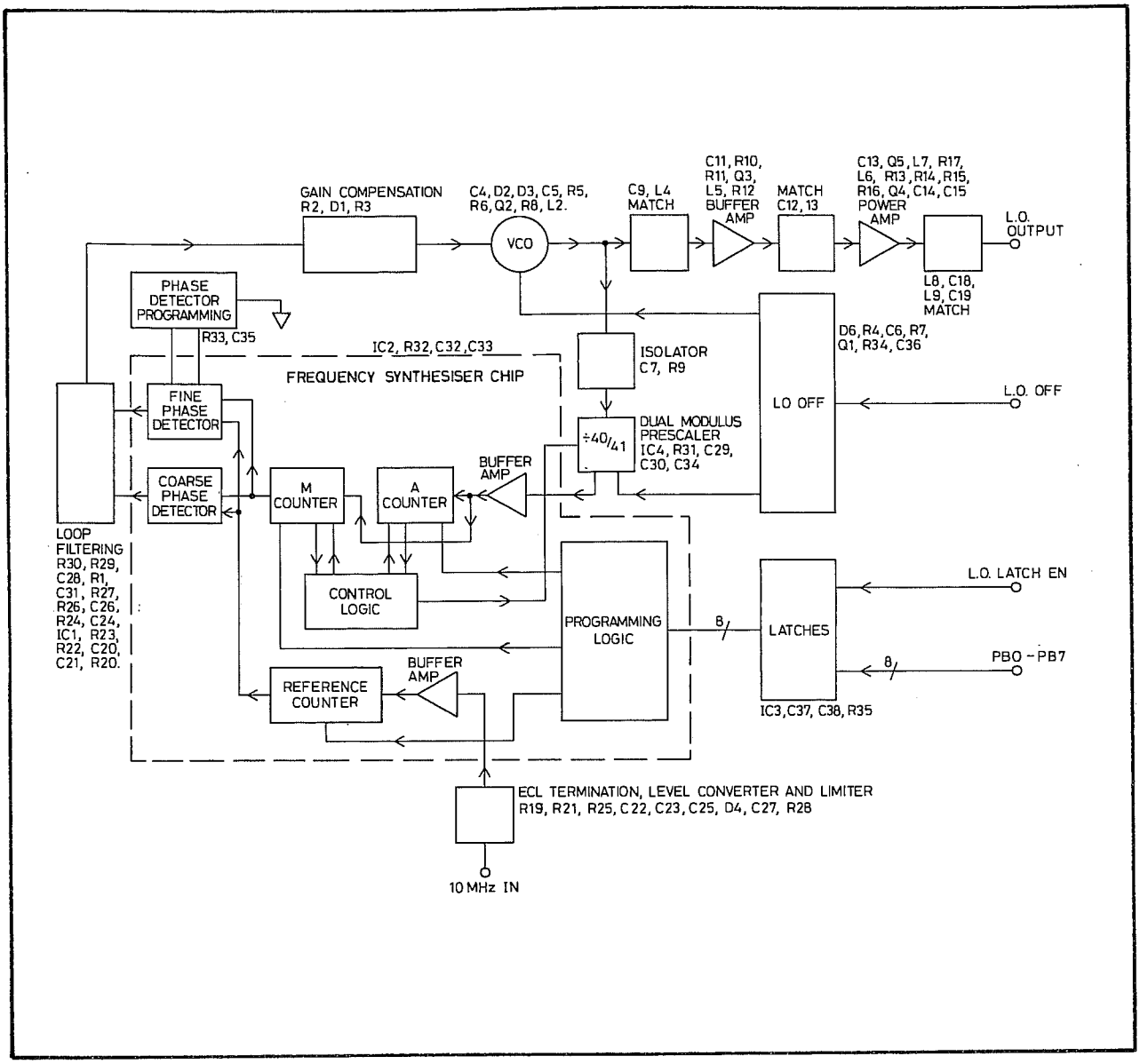


Fig. 6.6 LO Board Block Diagram

45 The reference frequency is divided down to form a PSD comparison frequency of 100 kHz. The required VCO frequency is also divided down to 100 kHz. A number of circuits are involved in this process, these are:

(1) A dual-modulus divider which will divide by one of two numbers, (N or N + 1), i.e. 40 or 41.

(2) An 'A' counter which is programmable and whose output controls the modulus of the divider.

(3) An 'M' counter which is programmable, is clocked in parallel with the 'A' counter. The output of the 'M' counter resets both itself and the 'A' counter.

46 The counters may count down to zero from the programmed number, or up from zero.

47 The 'A' counter is programmed to a number smaller than the 'M' counter. With both counters empty, the system starts with the divider dividing by 41. This continues until the 'A' counter reaches its pre-programmed value, then it causes the divider to divide by 40 until the 'M' counter is full. At the time the divider starts dividing by 40, the 'M' counter receives 'A' pulses, then the 'M' counter overflows M - A pulses later. The system spends 'A' cycles dividing by N + 1 and M - A cycles dividing by N. The total division ratio 'D' is given by:

$$D = A(N + 1) + (M - A)(N) = NM + A$$

48 In this way the 'M' counter gives coarse control of the total division ratio, whilst the 'A' counter provides minimum step size control.

49 The PSD produces an error signal proportional to the frequency/phase error between its two inputs. This error signal is passed through an integrator and applied to the VCO as a negative feedback tuning correction voltage. The system, therefore, maintains essentially zero phase error between the VCO output and the time base reference.

50 The output of the VCO is amplified to a nominal +23 dBm and is fed via a coaxial connector to the sampling mixer.

Circuit Description

51 For descriptive purposes the circuit description is split into two parts, the synthesizer and the output amplifier. Refer to Fig. 16 in Section 8 of this manual.

The Synthesizer

52 The VCO comprises Q2, D2, D3, PRINTED WIRING inductor and associated components. A positive increase in tuning voltage at L2 results in an increase in frequency.

53 The VCO output at Q2 collector is sampled by C7 and fed via R9 to the input of IC4, a divide by 40/41 dual modulus prescaler. IC4 divides down the VCO output to a frequency low enough to be handled by the main synthesizer chip, IC2. A block diagram of IC2 is given in Fig. 6.7.

54 The prescaled VCO frequency is fed to IC2/4. The signal is then further divided down by the 'A' and 'M' counters, which are programmed by the microprocessor according to the required LO frequency. The output of these counters is fed to one input of a coarse phase/frequency detector (PDB), and one input of a fine phase detector (PDA). The other, reference, inputs of these detectors are fed with 100 kHz, derived by dividing down the 10 MHz reference present at IC2/7 via a further internal programmable divider.

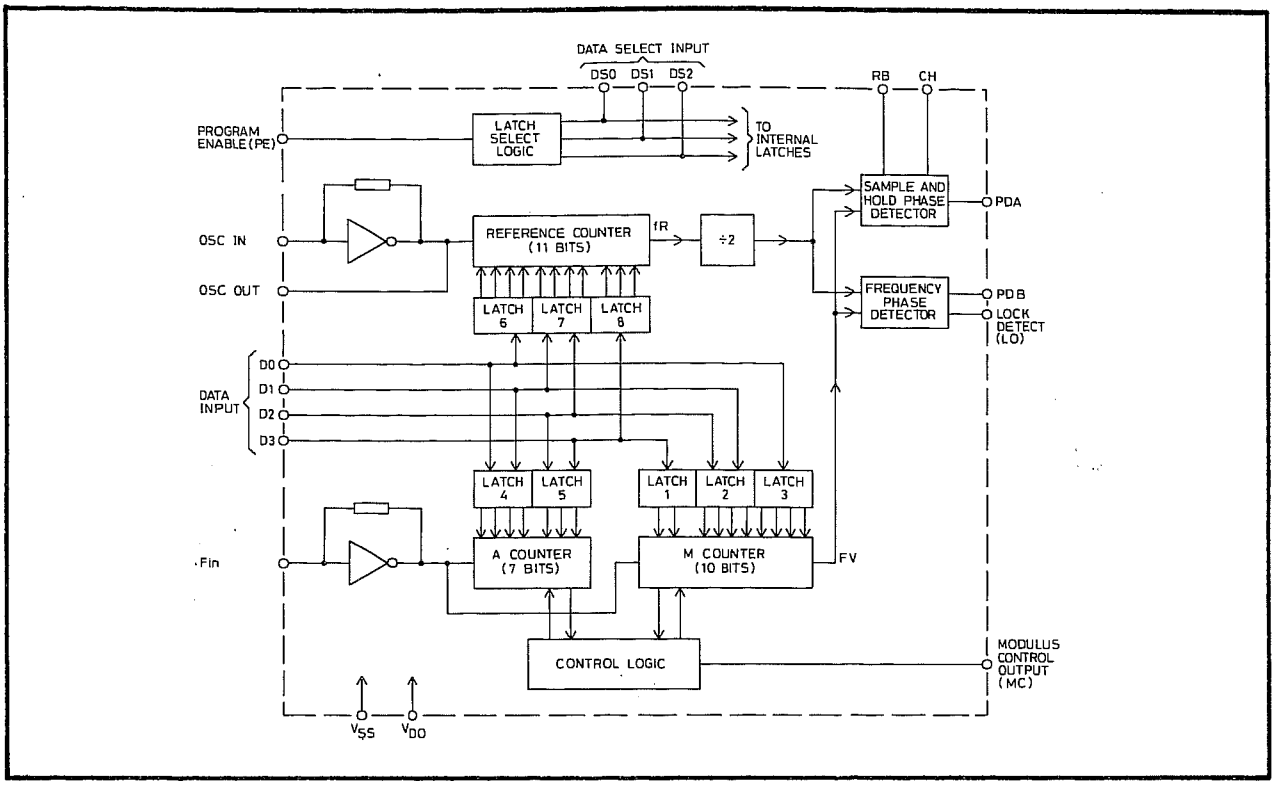


Fig. 6.7 Synthesizer IC2 Block Diagram

55 A large frequency/phase difference between the two inputs of PDA and PDB will result in PDA being inhibited and pulses proportional to the phase error appearing at PDB output. These pulses occur at a 100 kHz rate and are fed to the loop integrator comprising IC1, R1, C31, R27, C21 and R20. This integrator smooths and filters the pulsed output from PDB to form a cleaned correction voltage at IC1/6. This voltage is applied to the VCO as the tuning voltage via R2, R3 and L2. It's action is to force the VCO frequency and phase to a point where PDB, which has a tri-state output, goes high impedance and PDA takes over control.

56 PDA is a sample-and-hold fine phase-detector which produces an analogue correction voltage proportional to phase error. This voltage is fed to the loop integrator comprising R30, C28, R29, IC1, C21 and R20. The resulting voltage at IC1/6 pulls the VCO into phase lock with the 10 MHz reference.

57 D1, R2 and R3 provide a degree of loop gain compensation for higher VCO tuning voltages. R33 is a gain programming resistor, and C35 is an external hold capacitor for the sample and hold fine phase detector PDA.

58 R32 provides protection for IC2 in the event of a circuit malfunction elsewhere causing IC2 to latch up. C32 and C33 provide IC2 supply filtering. R31, C29, C30 and C34 provide IC4 supply filtering.

59 R19, R21, R25, C23 and C25 provide an ECL termination for the reference input at PL8. C22 is a DC block. D4a, D4b, R28 and C27 act as input protection for the OSC terminal of IC2.

60 R22 and C20 provide IC1 supply filtering. R23 is a programming resistor for IC1. R24 and R26 set the operating point of IC1 at approximately mid-way on the output swing of IC2 PDA and PDB. C24 and C26 provide filtering.

61 The internal 'A' and 'M' counters and the reference divider of IC2 are programmed by the microprocessor by means of data select lines DS0 to DS2, data input lines D0 to D3, and the program enable or strobe line PE. A logic 1 on the PE line transfers data from the data input lines to the internal latch selected by the data select lines, while a logic 0 disables the data input lines. Data transfer from all internal latches into the counters themselves, occurs simultaneously with the transfer of data into latch 1. Hence this is always the last piece of data sent by the microprocessor.

62 LO Off Control (PL35/2). A logic '1' on this pin forward biases D6a and D6b. This has two effects. One effect is that Q1 is switched on via R4, this removes Q2 base bias and inhibits oscillation of the VCO. The second effect is that IC4/5 is biased via R34 so that it will not self oscillate without applied VCO input.

63 Data Latch. A logic '0' on the 'LO LATCH ENABLE' line enables data present on lines PB0 to PB7 to be routed through IC3 to IC2. When 'LO LATCH ENABLE' is at logic '1', the data on those lines is latched at IC3 outputs. This action allows IC2 to work via a common 8-bit data bus, and also inhibits interference from microprocessor generated noise.

The Output Amplifier

64 The VCO output at Q2 collector is fed via matching network C9, L4 and C11 to the self bias amplifier stage comprising Q3, R11, R10, L5 and R12. The output of Q3 is fed via matching network C12 and C13 to a class A amplifier comprising Q5, L7 and R17. Components Q4, R13, R14, R15, R16 and C14 form an active bias circuit that keeps Q5 running at a constant collector current. R14 is a level control for adjusting Q5 collector current. The output of Q5 is fed via a matching network comprising C15, L8, C18, L9 and C19 to the LO OUTPUT at PL33. L6, C16, C17, L3, C8 and C10 provide supply filtering for the output amplifier.

THE IF PROCESSOR

Functional Description

65 The IF processor contains most of the IF conditioning circuits for selecting the appropriate IF from the sampler during acquisition, and converting the signal to a countable form. A small part of the IF conditioning circuit is also contained within the sampler module 17- 1102 and on the motherboard 19-3022. The sampler module is a sealed, non-user-serviceable item. A block diagram of the IF Processor is given in Fig. 6.8.

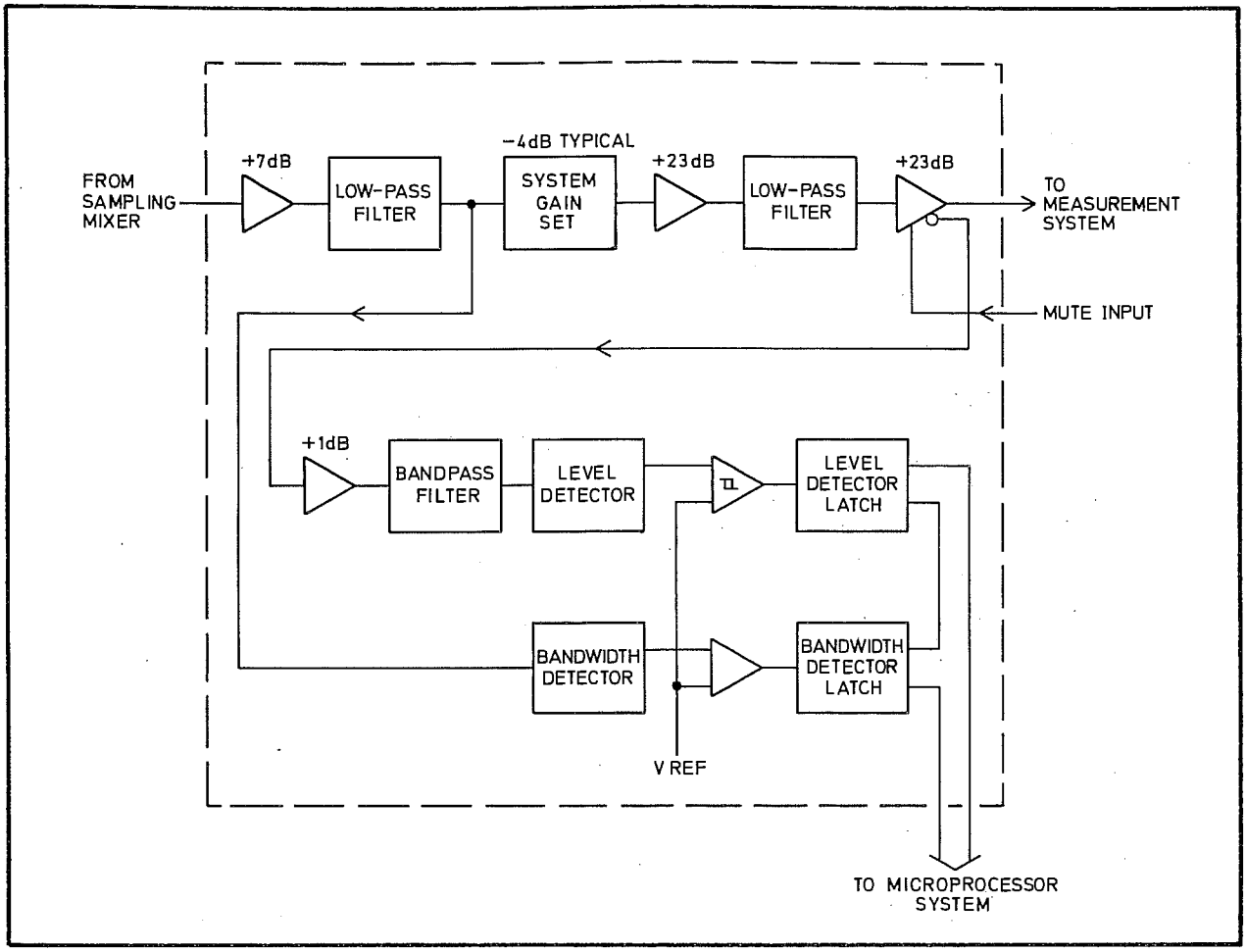


Fig. 6.8 The IF Processor

66 The IF output of the sampling mixer is first fed to an amplifier and filter combination. This provides IF gain and LO feedthrough attenuation. The signal is then fed to an adjustable attenuator that sets the overall system gain.

67 Two high-gain differential amplifiers with interstage filtering follow the attenuator. These stages amplify small signals and limit cleanly on large inputs. They ensure that the largest IF signal is the one that is counted. The second of the two differential amplifiers has two outputs. One output is fed to the motherboard where it is counted. The other output is fed via a buffer stage and bandpass filter to the level detector.

68 The band-limited level detector is used during acquisition to select the correct LO and IF frequency. It is also used to signal to the microprocessor that a signal is too small to be reliably counted.

69 A MUTE input is provided to disable the output from the IF processor. A bandwidth detector is included to help in calibration of one of the filters.

Circuit Description

70 Refer to the circuit diagram in Fig. 14 in Section 8 of this manual.

71 The IF output of the sampler module is fed to PL39. This is a dual function port. PL39 primarily accepts IF inputs from the sampler, it also feeds a DC bias current to the sampler module. This bias current is derived from the constant current source Q1 with R1, R2 and R3. R4 assists RF isolation and C2 and C4 provide decoupling. The IF input at PL39 is fed via C3 to the first gain stage comprising Q2, R5 to R10, C5 and C7. L1, C8 and C9 provide supply filtering.

72 The output of Q2 is fed via C6 to the 175 MHz low-pass filter (LPF) comprising L2, L3 and C10 to C15. C13 provides adjustment for the stopband edge. Detector D1 is provided to facilitate adjustment of C13.

73 The output of the 175 MHz LPF is fed to the variable attenuator R14 and R15. R14 provides adjustment of the system gain. R13 assists in providing the correct termination for the LPF.

74 The output from the wiper of R14 is fed to the differential amplifier comprising Q3 to Q6, R16 to R34, C18 to C30, and C32. This provides high gain and limits large input levels cleanly. This characteristic of the stage enables the instrument to discriminate against IFs other than the dominant one.

75 Following this first differential amplifier is a 200 MHz LPF comprising L4, L5, C31, C33 and C34. This reduces out-of-band noise thus improving the signal to total-noise ratio.

76 The output of the 200 MHz LPF feeds the second differential amplifier comprising Q8, Q10 to Q12, R37, R39, R41 to R43, R45 to R57, C38 to C50, and C52. This amplifier provides additional high gain with clean limiting.

77 This second differential amplifier provides two outputs. One output is fed to PL6 as 'IF COUNT', and it is this signal that is counted after further processing on the motherboard. The other output provides the level detector signal.

78 This second output is fed via buffer stage Q13, R59 to R64, C53 and C54 to the 31 MHz to 122 MHz band-pass filter (BPF) comprising L6 to L8, and C55 to C63. C61 is fitted as required to provide adjustment of the upper stop-band edge. The output of this filter is fed to the threshold detector comprising D2, D4, R65 to R71, and C64 to C66.

79 Comparator IC2b compares the output from D4a with the output from reference diode D4b. The output of IC2b 'IF LVL' is a logic '1' if an IF of sufficient amplitude is within the range 31 MHz to 122 MHz, or a logic '0' otherwise.

80 This data is also available in a latched form at IC1/8 as NOT 'IF LVL LCH', with reset via PL34/6 NOT 'IF LVL RST'. D2, R66, R68 and Q14 form a constant current source to forward bias D4a. R70 provides adjustment of the detector threshold point by varying the amount of bias current available to D4a. D4b provides basic temperature compensation for D4a. D2a and D2b compensate for small changes in amplifier gain that occur with temperature by slightly altering the bias current available to D4a, thereby adjusting its threshold point.

81 Comparator IC2a compares the output of D1a with its temperature compensating reference D1b. This provides the 'IF BW' output which is logic '1' if the cut-off frequency of the 175 MHz LPF is adjusted correctly or too high. This output is logic '0' if the cut-off frequency is set too low, (refer to the appropriate calibration section for full details of the use of this facility). The latch comprising IC1a and IC1b provides a NOT 'IF BW LCH' output with reset NOT 'IF BW RST'.

82 The 'IF COUNT' output can be muted. The mute request is received as a logic '1' at PL34/15 which turns Q7 off, therefore turning Q9 off. This removes the negative supply to Q8 and Q12, thus inhibiting the output from the final differential amplifier stage.

THE MEASUREMENT SYSTEM

Functional Description

83 The measurement circuits of the instrument are provided by three custom-built assemblies. These are two Multiple Counter and Control integrated (MCC) circuits, MCC1 and MCC2, and the Time Error Correction (TEC) hybrid H1. A block diagram is shown in Fig 6.9.

84 The process of counting involves the use of configuration circuits, count registers and interface circuits. These are contained jointly within MCC2 and MCC1. MCC2 contains the high-speed configuration and count register circuits. MCC2 also contains interface circuits to enable it to communicate with MCC1. MCC1 contains the low frequency configuration and count register circuits, it also contains count registers dedicated to handling the output from the TEC hybrid. MCC1 also contains interface circuits to enable it to communicate with MCC2 and the microprocessor system.

85 The circuits within MCC1 and MCC2 are configured by the microprocessor according to the measurement function in use. The counting process uses an enhanced recipromatic technique. The microprocessor selects an appropriate gate time based on the resolution selected. At the start of this gate time an EVENTS register is armed to start totalizing input cycles (events), starting with the next event. This register then proceeds to totalize the number of events occurring during the gate time. At the end of the gate time the EVENTS register is armed to stop totalizing, synchronous with the next event. This means that the EVENTS register only accumulates whole numbers of events.

86 A second register, called the TIME register, is connected to the 10 MHz timebase. This register is used to totalize the number of cycles of the timebase that occur while the EVENTS register is actually open. The first event to be accumulated in the EVENTS register arms the start of the TIME register, the very last event in the EVENTS register then arms the stop of the TIME register. This process is shown in Fig. 6.10.

87 The microprocessor reads the value of the EVENTS and TIME registers and divides EVENTS by TIME to obtain frequency. This is the basic reciprocatic technique which provides excellent resolution at low frequencies.

88 This resolution is further enhanced using Time Error Correction (TEC). Whilst the EVENT register always contains whole numbers of events, the TIME register may not contain whole numbers of time counts. This is because the first event, which arms the start of the TIME register may not be synchronous with the time counts. There could be a period of time between the arming of the TIME register and the occurrence of the first time count. This causes an error in the time count, which could be zero or as much as one clock period (100 ns). This can occur at the start and stop of the time count.

89 This time error is gated out as a pulse, and so that the following circuits do not have work down to 0 ns, an accurate 100 ns is added. This new pulse representing start or stop error plus 100 ns, is fed to the TEC hybrid which expands the total by a factor of 400 nominal. This expanded time is then counted using the 10 MHz timebase as a clock. The microprocessor then uses this count information to work out the original time error. The microprocessor calibrates the system during each measurement by applying accurate 100 ns and 200 ns pulses to the TEC circuits and noting the counts that result.

90 The outputs of INPUT A conditioner and INPUT B prescaler are fed directly to MCC2 for counting. The IF signal resulting from INPUT C, however, is divided by 2 before being fed to MCC2.

91 At the end of each measurement period, MCC1 generates an interrupt request for the microprocessor system. The registers within MCC1 and MCC2 are addressed using the address bus and the MCC SELECT line. The contents of the registers are transferred to the microprocessor system via the multiplexed bus.

92 The internal and external frequency timebase references (standards) are independently buffered, their outputs wire ORed. An external reference detector is included. The output of this circuit is used to inhibit the internal reference buffer whenever an external reference of sufficient amplitude is applied. The output of the wire OR gate is fed to MCC2, and the output of the external reference detector is fed to the microprocessor to signal when an external reference is in use. A 10 MHz output, derived from the frequency reference in use, is made available at a socket on the rear panel.

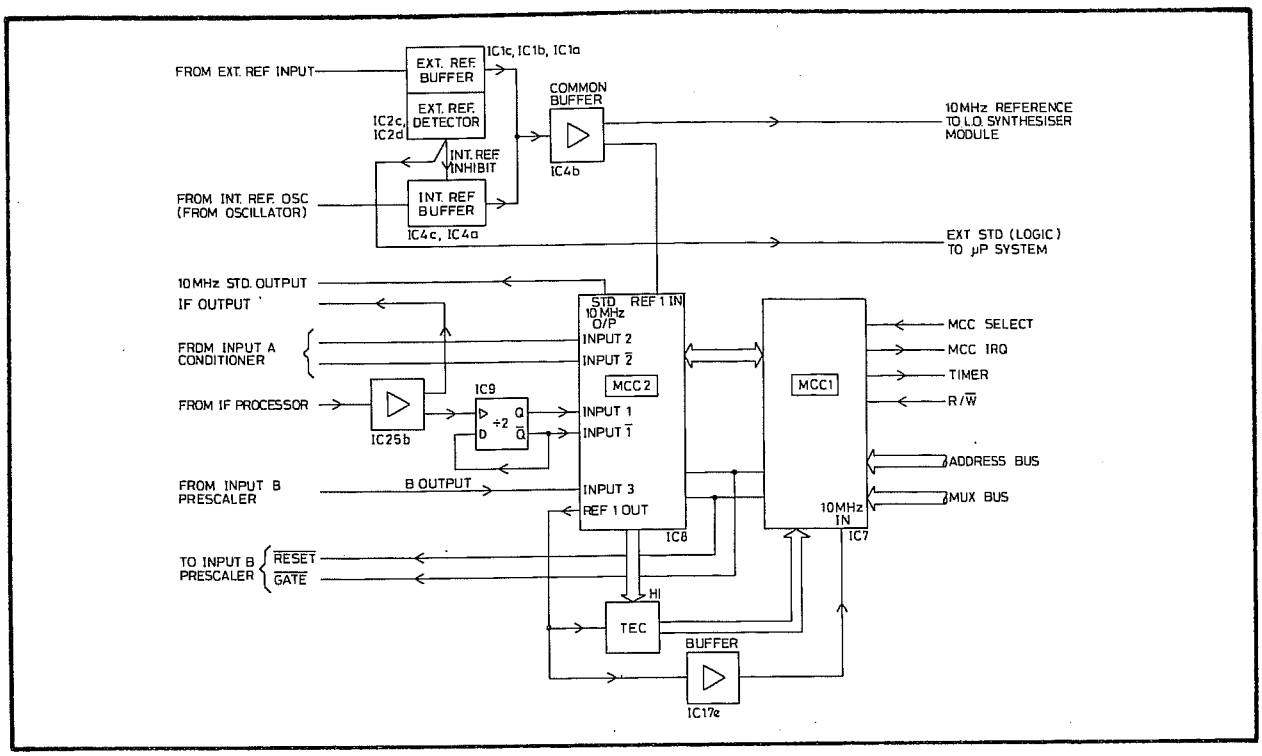


Fig. 6.9 The Measurement System

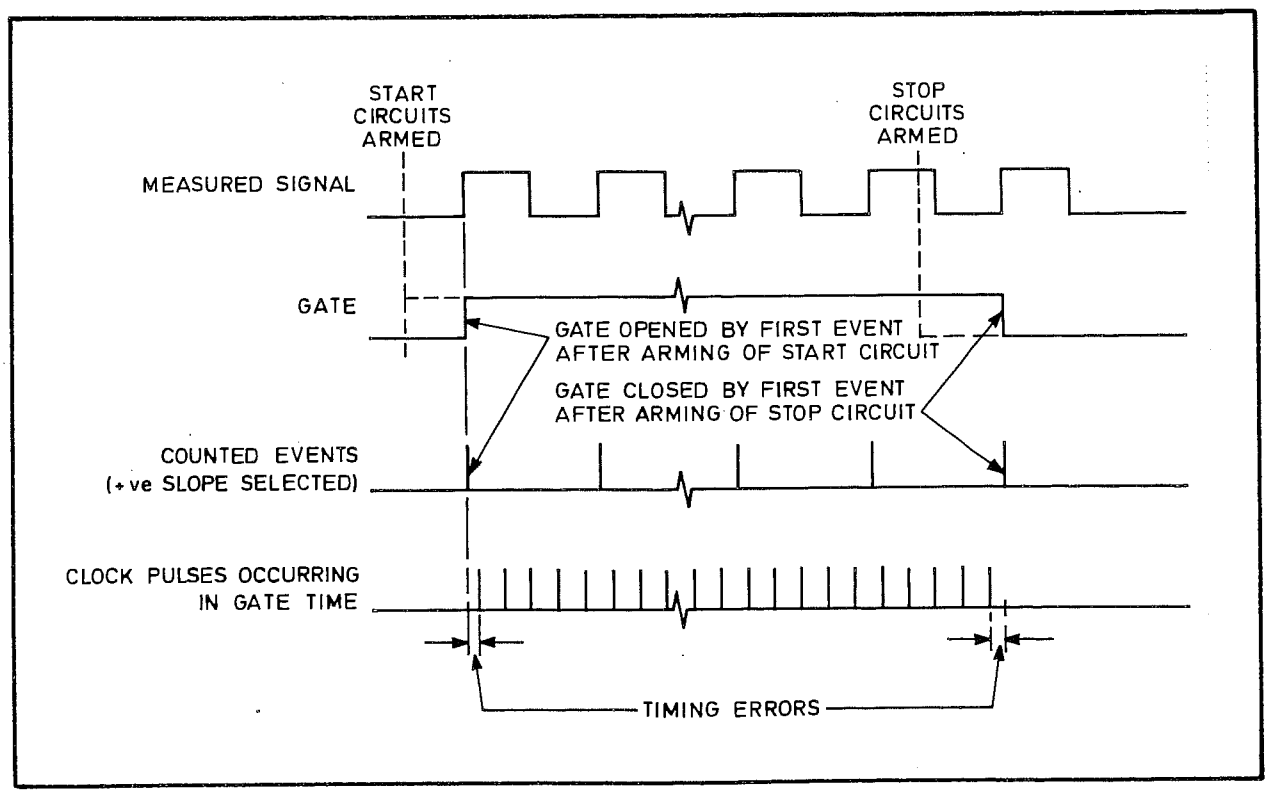


Fig. 6.10 Basic Reciprocatic Counting Technique

Circuit Description

93 The circuit diagram is shown in Fig. 3 in Section 8.

Measured signal input

94 The differential ECL outputs from INPUT A system are connected to IC8/17 & 18 via 50 Ohms microstrips. R17, R18, R112 and R113 are ECL terminating resistors.

95 The ECL output from INPUT B system 19-3025 enters at PL7/5 and is fed to IC8/19. R19 is the ECL terminating resistor.

96 The output from the IF processor enters at PL37 and is fed via attenuator R70 and R115 to one input of the ground referenced comparator IC25b. R22 and R33 determine IC25b hysteresis.

97 IC25b has differential outputs. One output, at IC25b/15, is fed to the IF output on the rear panel via R30, D3, R31, R32, C25 and PL38. The other output, at IC25b/16, is fed via a 50 Ohms microstrip to IC9/6. IC9 is configured as a divide-by-2 circuit whose output is fed to IC8/19.

Reference Frequency

98 The internal and external frequency standards are separately conditioned and then wire ORed together. The external standard conditioner incorporates a detector which inhibits the internal standard conditioner whenever a suitable external frequency standard is present. The wire ORed output from these conditioners feeds the REF1 IN pin at IC8/2.

99 A buffered version of the frequency standard in use is present at IC8/37, and is fed to the 10 MHz STD OUTPUT connector on the rear panel via R27 and PL19/1.

100 A buffered version of the frequency standard in use is also present at IC8/36. This signal is applied to the TEC hybrid, H1/6, and, after inversion in IC17e, to IC7/24.

Microprocessor Clock and Timer

101 A 5 MHz clock signal for the microprocessor (and the GPIB microprocessor if fitted) is generated by crystal XL1 connected to the OSC2 and CLOCK connections at IC6/38 and IC6/39 (in the microprocessor system). The 5 MHz clock signal is also fed to the GPIB (if fitted) via buffer Q22 and SK4/24. A 39.0625 kHz clock signal for the microprocessor timer is taken from IC7/4.

Channel B Gate and Reset

102 A NOT GATE signal (logic '0' during the measurement period) and a NOT RESET signal (negative going pulse at the end of each measurement period) are taken from IC8/27 and IC7/40 and fed to the Channel B system via PL7/17 and PL7/15.

103 The NOT GATE signal is fed to the GPIB via IC17a, IC16a, IC16d and SK4/21. The same signal is fed from IC16a to the GATE LED Flasher circuit comprising Q6 and Q7, whose output is fed to the GATE LED in the display unit via PL2/11.

Control Signals

104 The logic levels on lines Q0 to Q4, between IC8 and IC7 are shown in Table 6.1. These levels are stable if:

(1) No signals are applied to any of the channel inputs

(2) Manual acquisition mode is selected on Channel C.

TABLE 6.1

Control Signals

Measurement	Control Line				
Function	Q0	Q1	Q2	Q3	Q4
FREQ A	1	0	0	1	0
FREQ B	1	1	0	1	0
FREQ C	1	0	1	1	0
RATIO B/A with SF91	1	1	0	1	1
Special Function 72	1	1	1	0	1
Special Function 73	1	1	1	0	0
Special Function 74	1	1	1	0	0
Special Function 75	1	1	1	0	0

NOTE: Special Functions 72 to 75 can only be active when CHECK is selected.

THE DISPLAY SYSTEM

Functional Description

105 A block diagram of the display system is shown in Fig. 6.11. The seven-segment display elements are multiplexed under the control of the display drivers. Other LEDs on the front panel (e.g. O/F, REM, ADDR, SRQ etc.) are held on or off by control signals from other systems within the instrument.

106 To update the display, the microprocessor selects the appropriate display driver, using the MODE 1 and MODE 2 control lines. A string of nine 8-bit words (a control word and eight data words) is then put onto the bus. Each word is entered into memory within the display driver under control of the STROBE signal.

107 The display driver puts the data words onto its output bus in turn. For each data word, the appropriate numeric indicator or group of LEDs is enabled by a signal on its control line.

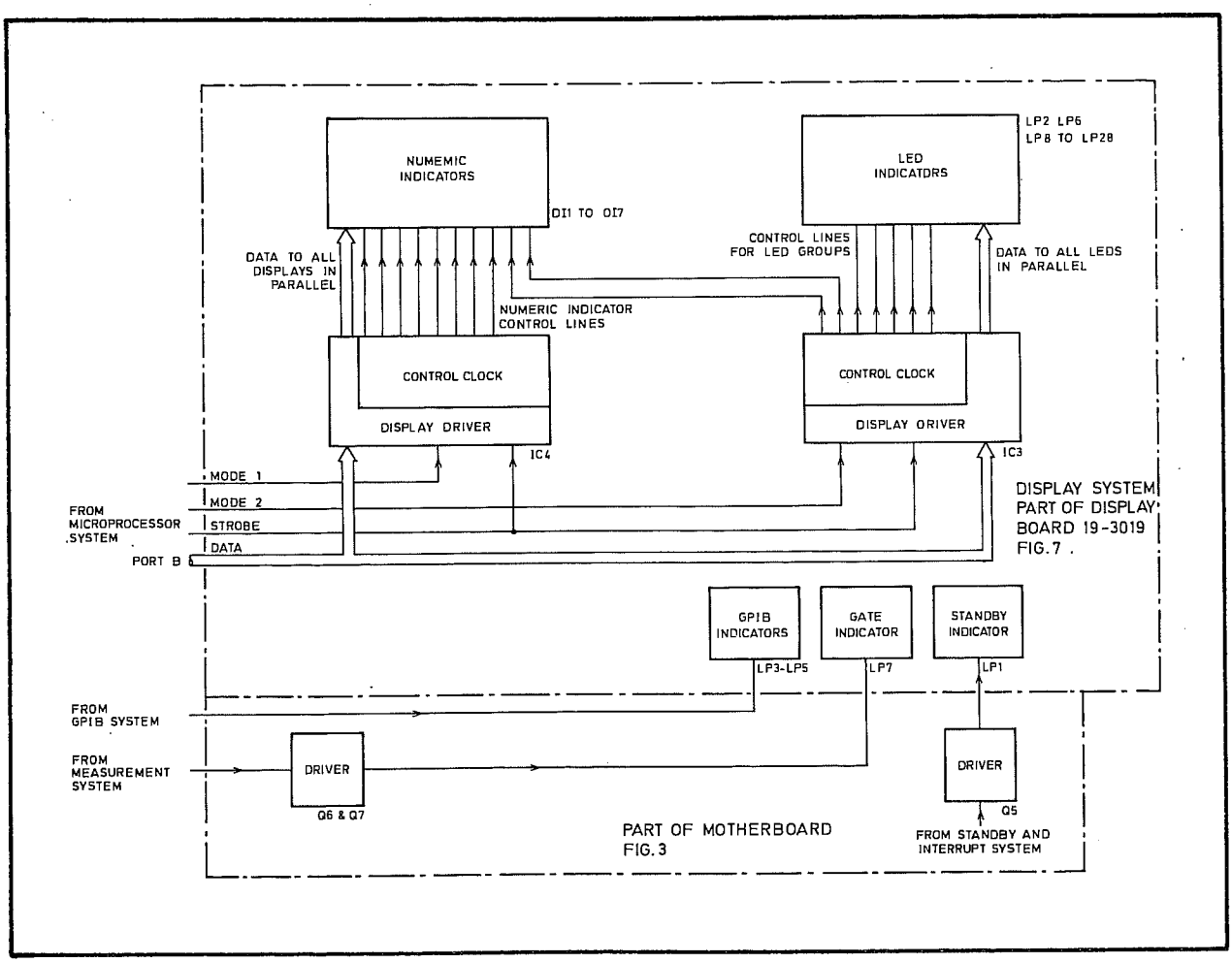


Fig. 6.11 The Display System

Circuit Description

108 The circuit diagram of the display system is shown in Fig. 7 in Section 8. The GPIB indicators, LP3, LP4 and LP5, are driven via SK1 from the GPIB system. The GATE indicator, LP7, is driven from the measurement system via a driver stage. The STANDBY indicator, LP1, is driven via SK1 pin 8 from the standby and interrupt system. The remaining LED indicators and the numeric indicators DI5-a to DI7 are controlled by the display driver IC3. Numeric indicators DI1-a to DI4-b are controlled by IC4.

109 Display data is stored in memory within IC3 and IC4. To change the data, the microprocessor puts a control word on the port B bus. The microprocessor writes this word into the display drivers by means of a negative pulse applied to the DISPLAY STROBE line at SK1 pin 4. The control word determines the operating mode of the display drivers.

110 The microprocessor then selects the display driver required by setting a logic '0' on the appropriate MODE line at SK1 pin 3 or pin 6. Eight words containing display data are written into the selected display driver via the port B bus, controlled by eight negative-going pulses on the DISPLAY STROBE line.

111 The output of each display driver is multiplexed, under the control of an internal clock. Eight-bit display data (for seven-segment plus decimal point or eight LED indicators) are put onto the device output bus (pins 1 to 4 and 24 to 27). A positive pulse is then applied to the enable line of the device or group of indicators which is to display the data. The enable line waveforms consist of 500 us positive-going pulses at approximately 250 pps.

THE KEYBOARD SYSTEM

Functional Description

112 A block diagram of the keyboard system is shown in Fig. 6.12. Encoding of the keyboard data is performed within the system without microprocessor action. An interrupt request (IRQ) is made on the KEYBOARD DATA ready line, to the microprocessor when encoding is complete. Data transfer is initiated by the KEYBOARD ENABLE active low signal from the microprocessor.

113 The keys are arranged into one 16-key and one 2-key matrix. When a key is pressed, its position is encoded into a 5-bit word. One bit, carried on the KEYBOARD EXTEND line, indicates the matrix in which the key is located. The remaining bits indicate the position of the key within the matrix.

114 When a key is pressed the encoder examines both matrices simultaneously, and generates a 4-bit code representing the key position. The same four bits are generated regardless of the matrix in which the keys are located.

115 If the key pressed is in the extended key matrix, the matrix input to the NAND gate is pulled low. The KEYBOARD EXTEND (active low) line is set to logic '0'. If the key is in the non-extended matrix the input to the NAND gate is isolated by the diode in that line, and the KEYBOARD EXTEND remains at logic '1'.

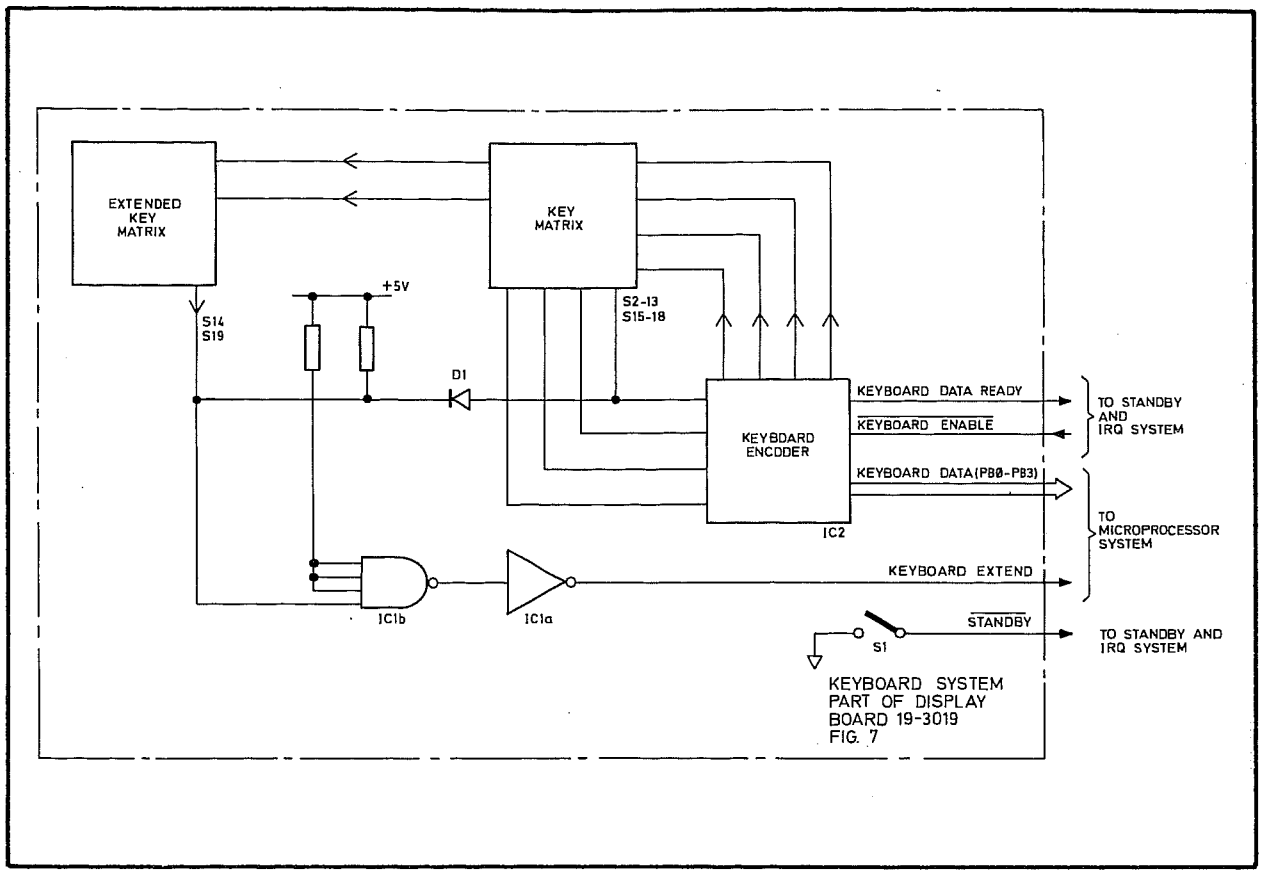


Fig. 6.12 The Keyboard System

Circuit Description

116 The circuit of the Keyboard System is shown in Fig. 7 in Section 8.

117 The keys are divided into two matrices (one 16-key and one 2-key), having common row lines connected to the encoder at IC2/7, 8, 10 and 11. The 16-key non-extended matrix column lines are connected to IC2/1, 2, 3 and 4. The 2-key extended column line is connected to IC2/1 via isolating diode D1.

118 The encoder normally holds the row lines at logic '0'. When a key is pressed the corresponding column line is pulled down to logic '0'. The encoder then scans the keyboard and stores a 4-bit code, corresponding to the row and column of the key, in an internal register. If a key connected to IC2/1 is pressed the encoder cannot find which matrix contains the pressed key.

119 The KEYBOARD EXTEND line indicates which matrix contains the key that is pressed. The inputs to IC2 are normally held at logic '1', so that SK2 pin 9 is at logic '1'. If a key is in the extended matrix is pressed, the input on IC1-b/12 is pulled to logic '0' and SK2 pin 9 will go to logic '0'. The column line of the non-extended matrix connected to IC2/1 is isolated from IC1-b/12 by D1, so that the logic level at SK2 pin 9 is not changed when a key in this matrix is pressed.

120 When the key-position code has been stored, the encoder sets the KEYBOARD DATA ready line, at SK2 pin 4, to logic '1' giving a microprocessor interrupt. The microprocessor sets IC2/13 to logic '0' using the KEYBOARD ENABLE (active low) line, and the encoder puts the 4-bit code onto the bus. The microprocessor reads the code and the state of the KEYBOARD EXTEND line to find which key has been pressed.

THE MICROPROCESSOR SYSTEM

Functional Description

121 A block diagram of the system is shown in Fig. 6.13. The microprocessor used has a 5-bit bus for the high-order address bits and an 8-bit multiplexed bus which is used for the low-order address bits and for data. The low-order address bits are strobed into the address latch, which holds them on an 8-bit address bus, to free the multiplexed bus for data.

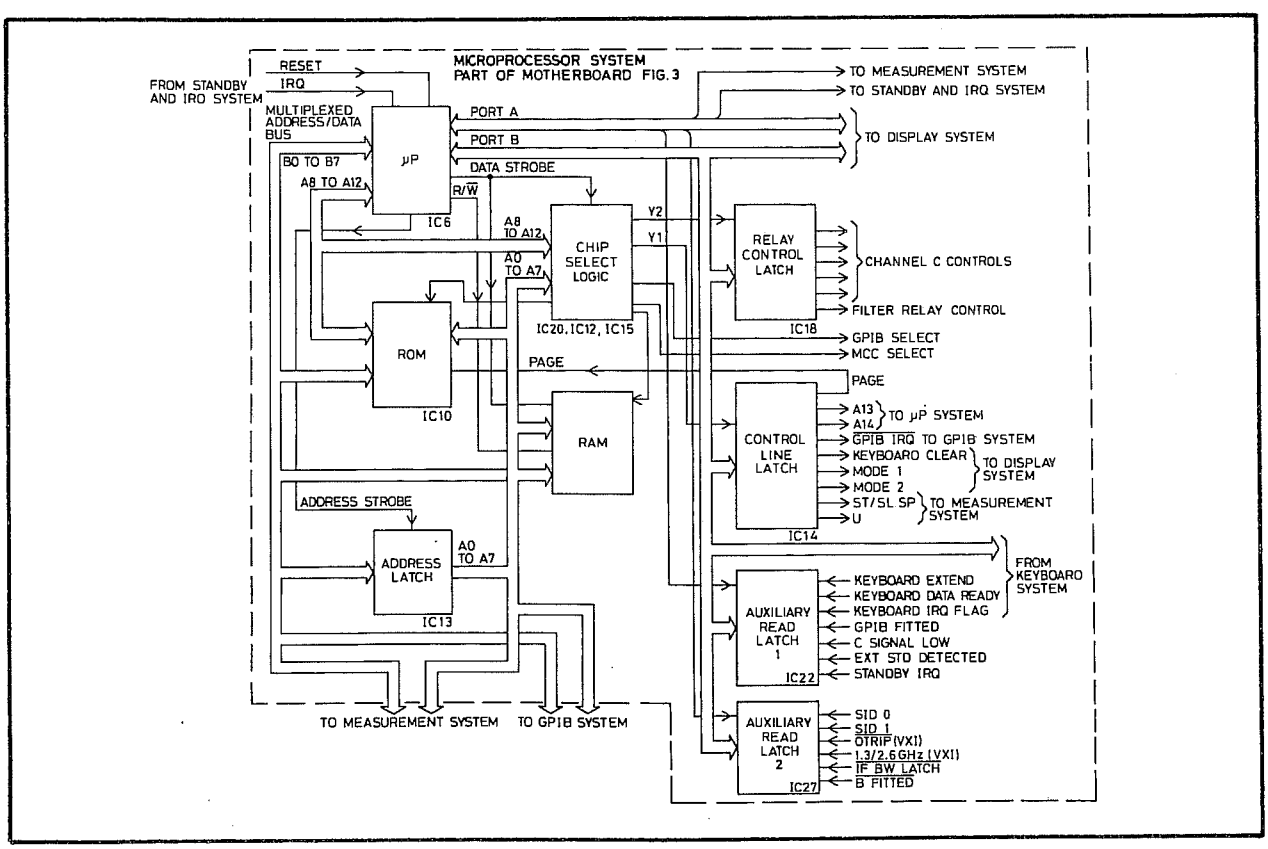


Fig. 6.13 The Microprocessor System

122 Two latches fed from Port B of the microprocessor, are used to maintain voltage levels on the instrument control lines. Two buffers are used to read the status of the instrument flags via Port B. The latches and registers for the connection of the multiplexed bus to the measurement system are in the measurement system, and are controlled by the MCC SELECT signal. The display data latches are in the display system, and are controlled by strobe and chip-select signals obtained from Port A.

Circuit Description

123 The circuit diagram is given in Fig. 3 in Section 8. The microprocessor timer signal is generated in the measurement system and is fed to IC6/37. The 5 MHz microprocessor clock is generated by XL1 and circuitry within IC6 connected to IC6/38 and IC6/39. The 5 MHz clock signal is also fed to the GPIB (if fitted) via buffer Q22 and SK4/24. A NOT RESET signal is generated in the Standby and IRQ System when the instrument is switched on or off, this is fed to IC6/1.

124 The microprocessor bus for the high-order address bits is designated A8 to A12. The multiplexed bus, used for the low-order address bits and for data is designated B0 to B7. The microprocessor also has two input/output ports PA0 to PA7 and PB0 to PB7.

Multiplexed Bus Operation

125 The microprocessor puts IC6/6 (ADDRESS STROBE) to logic '1' and IC6/4 (DATA STROBE) to logic '0'. This enables the address latch, IC13 (IC13/11 at logic '1'), and disables the address decoder, IC15 (IC15/6 at logic '0').

126 The address is put onto lines B0 to B7 and A8 to A12. When the lines have settled the ADDRESS STROBE line is taken to logic '0'. The low- order bits of the address are latched into IC13, and are held on address lines A0 to A7. Lines B0 to B7 are now free for use as a data bus.

Address Decoding

127 The levels on address lines A6 to A12 are decoded in IC15 to provide the following outputs:

(1) NOT MCC SEL, the chip-select signal for IC7.

(2) NOT GPIB SEL, the chip-select signal for the GPIB address decoder.

(3) Y1, the chip-select signal for output latch IC14.

(4) Y2, the chip-select signal for output latch IC18.

128 These outputs are only available when IC15 is enabled by a logic '1' at IC15/6 and a logic '0' at IC15/4 and 5. The level at IC15/6 is set by the DATA STROBE output at IC6/4, which is logic '1' when the multiplexed bus is available for data transfer. All outputs from IC15 are decoded from addresses with lines A9 to A12 at logic '0', when IC15/4 and 5 are held at logic '0' by the Y3 output from IC12/12. This output is set by the output of IC20-b at logic '0' appearing at IC12/4 and 5, together with the decoded addresses with lines A7 to A9 at logic '0', at IC12/1, 2 and 3.

129 The levels on address lines A0 to A7 are decoded by IC5 to provide data at the B0 to B7 read/write ports of the RAM. This data transfer is only available when IC5 is enabled by a logic '0' at IC5/19 and 20 from IC16-c. IC5 is instructed to READ with a logic '1' at IC5/21 and to WRITE with a logic '0' at the same point, from IC6/5 together with the DATA STROBE output at IC6/4, both via IC19-a.

Input and Output Latches

130 The logic levels required on the instrument control lines and on the PAGE line (most significant bit of the RAM address) are set into the output latches, IC18 and IC14, from data Port B (PB0 - PB7) of the microprocessor. The latch strobe signals are decoded in IC15. Data may be read by the microprocessor from the input latch, IC22. The latch strobe signal is provided via Port A (PA0 - PA7) of the microprocessor.

THE STANDBY AND IRQ SYSTEM

Functional Description

131 The system generates reset signals for the microprocessor and GPIB interface, and the standby switching signal for the power supply system. It also combines the IRQ signals from the GPIB interface, the measurement system and the keyboard system for connection to the microprocessor. A block diagram is given in Fig. 6.14.

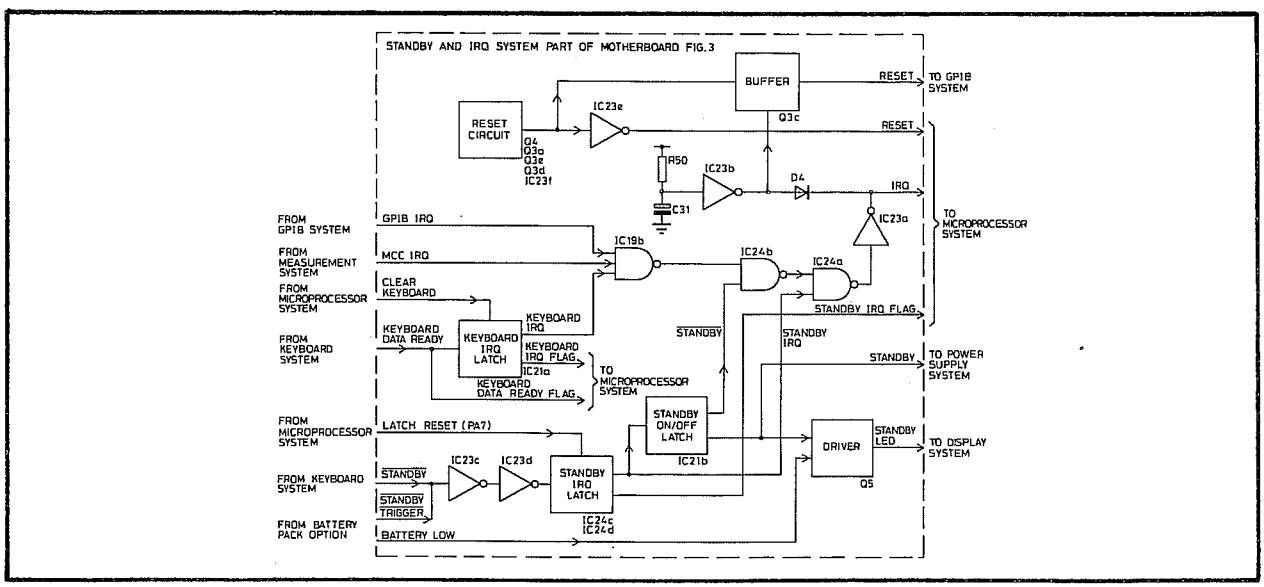


Fig. 6.14 The Standby and IRQ System

132 Reset signals for the microprocessor and the GPIB interface are generated whenever power is applied to or removed from the instrument's power supply system.

133 On switching to standby, the standby signal from the keyboard system sets the standby IRQ latch. The latch outputs provide the standby IRQ and standby flag for the microprocessor system. The standby IRQ output also clocks the standby ON/OFF latch to the set state. This provides signals to switch the power supply to standby, light the STANDBY indicator and disable IC24b, so inhibiting the other IRQs. At the end of the microprocessor interrupt routine the standby IRQ latch is reset, removing the standby IRQ. The state of the standby ON/OFF latch is not changed.

134 While the instrument is in standby, the input to IC23b is held low and the IRQ input to the microprocessor is held high via D4. This inhibits all IRQs. The output from IC23b also holds the GPIB interface reset via Q3c.

135 On return from standby, the standby IRQ latch is again set by the standby signal from the keyboard system. The standby ON/OFF latch is clocked to the reset state, the power supply is returned to normal operation and IC24b is enabled. The input to IC23b rises as C31 charges, removing the reset signal from the GPIB interface and enabling the microprocessor IRQ input. The microprocessor is now able to accept the IRQ from IC24a. At the end of the restart sequence the standby IRQ latch is reset.

136 When the encoder in the keyboard system has data ready to be read by the microprocessor, the keyboard IRQ latch is clocked via the KEYBOARD DATA READY line. The latch outputs provide the keyboard IRQ and a keyboard IRQ flag. Once the keyboard has been identified as the source of the interrupt, the latch is reset by the microprocessor.

Circuit Description

137 The circuit diagram is shown in Fig. 3 in section 8.

Reset Circuit

138 The NOT RESET signal is generated in the circuit containing Q4, Q3a, Q3d, Q3e, and C30. When the instrument is switched on, the input to IC23f is held low until C30 charges through R44, Q3a and R47. The output at IC23f/12 goes to logic '1' when power is applied, but drops to logic '0' after approximately 300 ms. This output is inverted by IC23e to provide the microprocessor reset and by Q3c to provide the GPIB reset.

139 If there is a reduction in the +5 V STANDBY supply, due to the instrument being switched off or to power failure, the potential across R45 falls. The potential at Q4 emitter is maintained by the charge in C30, so Q4 conducts. The current in R46 makes the base of Q3d positive, so the transistor conducts and holds the base of Q4 low until C30 is completely discharged. This ensures that a good reset action is obtained, even if the power is quickly restored.

Standby Operation

140 On switching to standby, PL1 pin 14 is taken to 0 V by the STANDBY key. Debouncing is provided by R37 and C27. The leading edge of the signal is sharpened in IC23c, C28, R36 and IC23d, and sets the standby IRQ latch, IC24c and d.

141 The negative-going output from IC24c/10 is passed via IC24a, IC23a and R49 to IC6/12, to provide a microprocessor interrupt. The positive-going output from IC24d/11 forms the standby IRQ flag (read by the microprocessor via IC22 during the interrupt routine) and clocks the standby latch, IC21b, to the set state.

142 The logic '0' level at IC21b/8 switches on Q5, and provides power for the STANDBY indicator via PL1 pin 8. The same output is applied to IC24/5, and disables the other interrupts, which are connected to IC24b/6.

143 The logic '1' level at IC21b/9 shuts down the power supplies except the +5 V STANDBY supply.

144 At the end of the interrupt routine the microprocessor resets the standby IRQ latch by applying logic '0' to IC24c/8 from IC6/7.

145 On return from standby, the standby IRQ latch is again set. This provides a microprocessor interrupt and sets the standby IRQ flag, as before. The positive-going output from IC24d/11 clocks the standby latch to the reset state, so that the STANDBY indicator is turned off and the power supplies are restored. The microprocessor resets the standby IRQ latch at the end of the interrupt routine.

146 When the instrument is operating from the battery pack in the battery-save mode, the NOT STANDBY TRIG control line (PL21 Pin 8 on Fig. 4) is taken to logic '0' after approximately one minute by the battery pack. This switches the instrument to the standby mode. The instrument is returned to the measurement mode by operation of the STANDBY key.

The IRQ Circuits

147 The KEYBOARD DATA READY line, at PL2 pin 4, goes to logic '1' when the keyboard encoder has data available. This clocks IC21a to the set state to provide a keyboard IRQ flag at IC22/11 and an interrupt signal at IC19b/9. Interrupts from the measurement system (NOT MCC IRQ) and the GPIB interface (NOT GPIB IRQ) are connected to IC19b/12 and IC19b/10 and 13.

148 If any of these interrupts occur, IC19b/8 and IC24b/6 will go to logic '1'. Provided the standby latch, IC21b, is not set, IC24b/5 will be at logic '1' and the interrupt signal passes via IC24a and IC23a to IC6/2.

149 When the instrument is switched into or out of the standby state, the standby IRQ latch, IC24c and d, is set. The standby IRQ from IC24c/10 is fed to IC6/2 via IC24a and IC23a.

150 The circuit comprising R50, C31, IC23b and D4 disables the microprocessor interrupt input and holds the GPIB microprocessor reset line low (via Q3c) while the +5 V power supply to R50 is switched off. On return from standby, C31 charges and IC23b/4 goes to logic '0'. The microprocessor interrupt input is enabled and the GPIB microprocessor is reset. The delay in enabling the interrupts prevents the standby IRQ which occurs on return from standby from being acted upon before the power supplies are fully restored.

THE POWER SUPPLY SYSTEM

Functional Description

151 A block diagram of the Power Supply System is shown in Fig. 6.15. The power supply is mounted wholly on the motherboard assembly. The power supply accepts a wide range of AC line supplies and provides the following regulated DC supplies:

(1) +15 V

(2) +12 V

(3) +5 V

(4) +5 VM

(5) +5 V STBY

(6) -5.2 V

152 The Battery Pack Option can also be fitted within the instrument and when installed is connected to the Power Supply System.

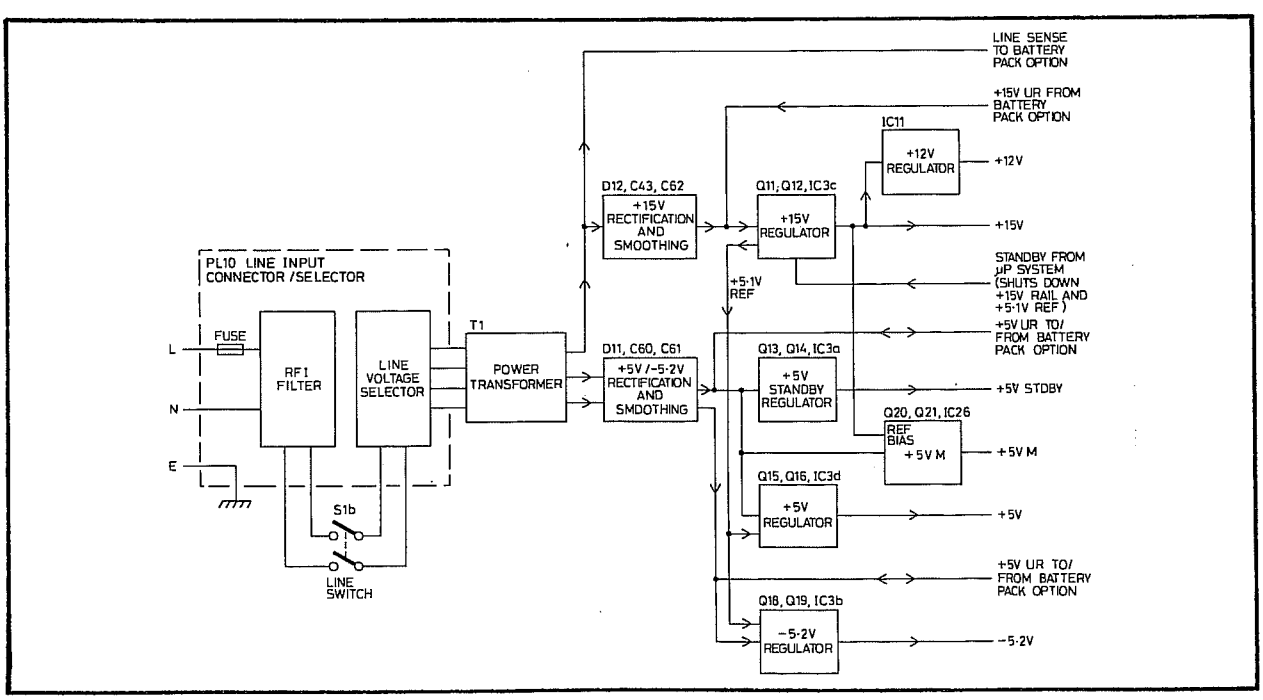


Fig 6.15 The Power Supply System

153 Conventional full-wave rectification and smoothing are employed, and the majority of the regulators are of a discrete, low drop-out design. The latter assures a high level of efficiency which is essential for both low temperature rise and for enhanced operation when running from the optional battery pack.

154 In standby operation the microprocessor shuts down all DC supply rails except for +5 VSTBY.

Circuit Description

155 The circuit diagram is shown in Fig. 4 in Section 8 of this manual. The AC supply enters the instrument at PL10. PL10 is a combined connector, fuse, RFI filter, line voltage selector unit mounted on the motherboard and protruding through the instrument rear panel. The output of the RFI filter and the input of the line voltage selector are linked externally via S1a and S1b. The output of the line voltage selector is connected to the primary windings of transformer T1.

156 The center-tapped secondary of T1 feeds the rectifier/filter circuit comprising D11, C60 and C61. This provides the unregulated DC rails +5 VUR and -5.2 VUR. The other secondary winding of T1 feeds the rectifier/filter circuit comprising D12, C43 and C62 to provide the +15 VUR rail.

157 Q13 and associated components comprise the +5 VSTBY regulator circuit. The output voltage at Q13 collector is fed to the inverting input of IC3a. The non-inverting input of IC3a is referenced to +5 V derived from D9. The output of IC3a constitutes an error voltage proportional to the difference between the +5 VSTBY output and the +5 V reference. This error voltage drives Q14 which in turn controls the base current of Q13 to reduce the error on the +5 VSTBY rail. R98e buffers the +5 V reference and C89 provides filtering. R98a and C50 are loop-stability components. Two other DC rails, +5 VSTBYD1 and +5 VSTBYD2, are derived from the +5 VSTBY rail via R109 and R110 respectively.

158 The +5 V regulator, comprising Q15 and associated components, is identical in operation to the +5 VSTBY regulator, except that the op- amp reference input is switchable to ground. This is done via Q17 which is controlled by the STDBY line from IC21/9.

159 The -5.2 V regulator, comprising Q19 and associated components, is identical in operation to the +5 VSTBY regulator except that its op- amp reference is 0 V and the op-amp feedback voltage is derived from the tap of a potential divider between the -5.2 V and +5 V outputs formed by R104a to R104e. When the +5 V rail is disabled during standby, the -5.2 V rail is also disabled.

160 The +15 V regulator, comprising Q11 and associated components, is identical in operation to the +5 V regulator, except that the op-amp feedback voltage is derived from the tap of the potential divider between +15 V and ground, comprising R77, R96 and R97. R77 provides adjustment of the +15 V rail. C91 improves noise rejection on the rail.

161 The reference voltage, applied to the regulator op-amps, is derived from D9 and is biased from the constant current source comprising Q10, R92, R93, R125 and D7.

162 The +5 VM rail is a very low noise rail which powers certain critical circuits in the LO synthesizer and IF processor. Operation of the +5 VM regulator, comprising Q20 and associated components, is identical in operation to the +5 VSTBY regulator, except that it has its own low noise reference voltage. This reference voltage is provided by D16, R153, R154, and C92 to C94. This reference circuit is biased from the +15 V rail. In standby mode the +15 V rail is disabled and, therefore, so is the +5 VM rail.

163 Both the +5 VM rail and the +15 V rail are filtered to provide the +5 VMF and +15 VF rails respectively.

Standby Mode

164 In standby mode all DC supply rails, except +5 VSTBY and its derivatives, are switched off (disabled). Selecting standby sets the output of latch IC21b/9 to logic '1' and switches Q17 on via R98c. This action reduces the reference voltage of the +5 V and +15 V regulators to zero. As the +5 V rail is disabled, so is the -5.2 V rail.

165 The fan power supply is derived from the +5 VSTBY rail. IC2b, Q8, Q9, R148 to R152 and R76 comprise the fan control circuit. This circuit inhibits fan operation when the instrument is powered from the optional battery pack (if fitted). Under these conditions the NOT 'FAN ON' line at PL21/12 is held high which causes the output of IC2 to go high. This action switches off Q8, which switches off Q9, and inhibits the fan.

THE FREQUENCY STANDARD SYSTEM

Functional Description

166 The internal frequency standards 19-1147 and 19-1208 are 10 MHz oscillators. Frequency standards 9423 and 9444 each comprise a 5 MHz oscillator and a frequency doubler. A block diagram of the 9423 and 9444 oscillators is shown in Fig. 6.16.

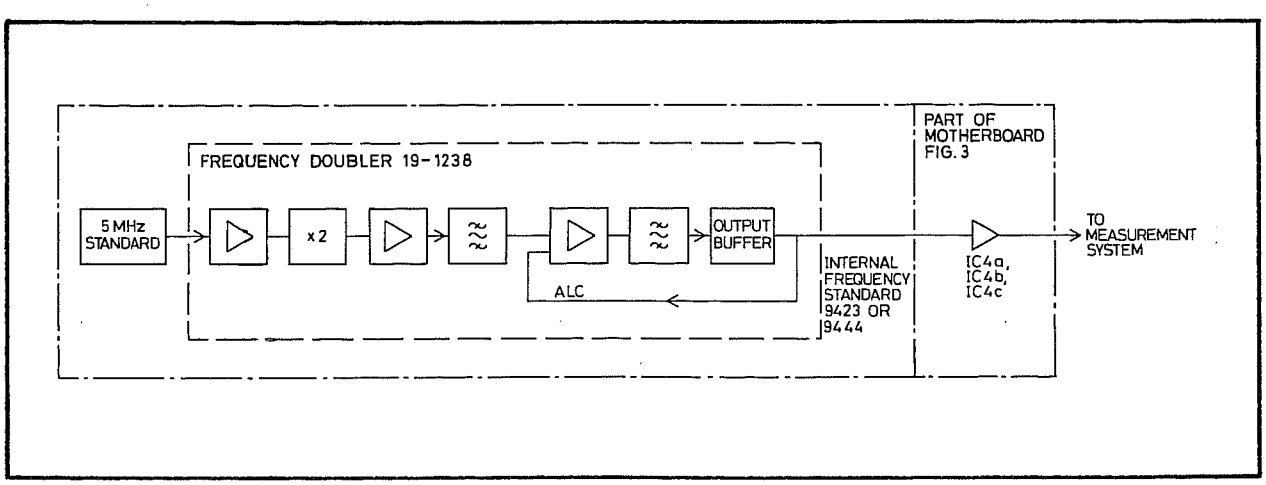


Fig. 6.16 9423 and 9444 Oscillators

167 For all the oscillator types the 10 MHz signal is passed to the measurement system via a buffer on the motherboard.

168 Signals from a suitable external frequency standard are applied to a signal conditioning/detection circuit. This circuit inhibits the internal standard and delivers a conditioned version of the external standard to the measurement system. For external frequency standards at sub-multiples of 10 MHz, the external frequency multiplier option is fitted between the conditioning circuit and the measurement system.

Circuit Description

Frequency Doubler

169 The circuit diagram of the frequency doubler, used with frequency standards 9423 and 9444, is given in Fig. 23 in Section 8. The 5 MHz input is applied to the balanced amplifier containing Q1 and Q2. The base of Q3 is driven by the differential outputs from the amplifier, via D1 and D2, so that the frequency here is 10 MHz.

170 The 10 MHz signal is amplified and filtered in the two stages containing Q3 and Q5, and fed to pin 3 Via the buffer, Q6.

171 The output signal is fed back via C6 to switch Q4 on during the positive peaks of the signal. The gain of Q5 is controlled by the potential across C3, which charges via R12 and discharges via Q4. If the output signal level increases, the time for which Q4 conducts increases so that the mean potential across C3 decreases. The resulting decrease in gain of Q5 provides automatic level control.

Internal Frequency Standard Buffer

172 The output from the internal standard oscillator enters at PL14/4, and is fed via C82, R142 and C83 to one input of a high gain comparator comprising IC4c and IC4a connected in tandem. R143 is a terminating resistor. R142 and D14 form a signal level clamp.

173 IC4 is an ECL triple line-receiver, which features a built-in reference bias, Vbb. The two inputs of IC4c/13 are biased to this Vbb reference via R144 and R147. Signal variations on IC4c/13 cause IC4/15 to toggle. R145 biases the ECL output, which is fed to IC4a/5. The output of IC4a/2 is wire ORed to IC1a/2 (via PL16/8 & 9 and LK1), and also feeds a further comparator IC4b. One of the differential outputs from IC4b forms the 10 MHz reference for the LO synthesizer, via PL30, while the other output is fed to the 'REF 1' input at IC8/2.

External Frequency Standard Buffer

174 The EXT REF input from the rear panel enters at PL20/4, and is fed via C71, R126 and C72 to one input of a high gain comparator comprising IC1c and IC1b connected in tandem (IC1 is a triple line- receiver). R127 is a terminating resistor. R126 and D5 form a signal level clamp.

175 The non-inverting inputs of IC1c and IC1b connect directly to Vbb, whilst the inverting inputs are biased via R128 and R131.

176 The output at IC1b/7 is configured as a signal presence detector. R132 biases the ECL output as normal, and C74 is a hold capacitor that acts with the emitter output to form a peak detector. IC1b/7 will be an ECL logic '1' if an external standard is present. This detector output is connected to a pair of comparators, IC2c and IC2d. The output of IC2d feeds an 'EXT REF PRESENT' signal via TTL level converter, R139 to R141 and D15, to the microprocessor system via IC22/6. The output of IC2c is connected via R146 to IC4a/4 and IC4c/12. With an EXT REF applied, IC2c will be low (-5.2 V), which biases IC4a and IC4c so that they no longer toggle, therefore, inhibiting the internal standard.

177 The output at IC1b/6 connects to comparator IC1a which has differential outputs. One output at IC1a/3 feeds an 'EXT REF -' signal to PL16/6, for use with the REF MULTIPLIER option, when fitted. The other output, at IC1a/2 is wire ORed to IC4a/2 (via PL16/8 & 9 and LK1).

178 In operation, since IC4a output is wire ORed to one output of IC1a, this node will carry either INT REF or EXT REF signals. It cannot carry both since the INT REF path is inhibited whenever an EXT REF signal is applied. Therefore, the outputs of IC4b will be either INT REF or EXT REF.

REFERENCE FREQUENCY MULTIPLIER (OPTION 10)

Functional Description

179 The block diagram of the multiplier is shown in Fig. 6.17. The input to the circuit is taken from the EXT STD INPUT connector on the rear panel, via a signal conditioning circuit on the motherboard. The output of the circuit is passed to the measurement system. The NOT BYPASS control line is held at logic '1' by the +5 V STANDBY supply.

180 The circuit contains a 10 MHz oscillator operating in a phase-locked loop. If an external reference signal of suitable amplitude is present at the EXT STD INPUT connector, a rectangular waveform at the reference frequency is fed to the external reference detector. The detector output triggers the switching signal generator. The oscillator is then enabled and the bypass logic connects the 10 MHz from the buffer and splitter to the output.

181 The pulse generator output is fed to the phase detector, and forms the reference signal for the phase-locked loop. The phase detector is of the sampling type, allowing the oscillator to be phase-locked to a reference signal of 10 MHz or any sub-multiple of 10 MHz.

182 If no external reference signal of suitable amplitude is present at the EXT STD INPUT connector, the reference detector output does not trigger the switching generator. The oscillator is disabled and the bypass logic connects the circuit input to the output.

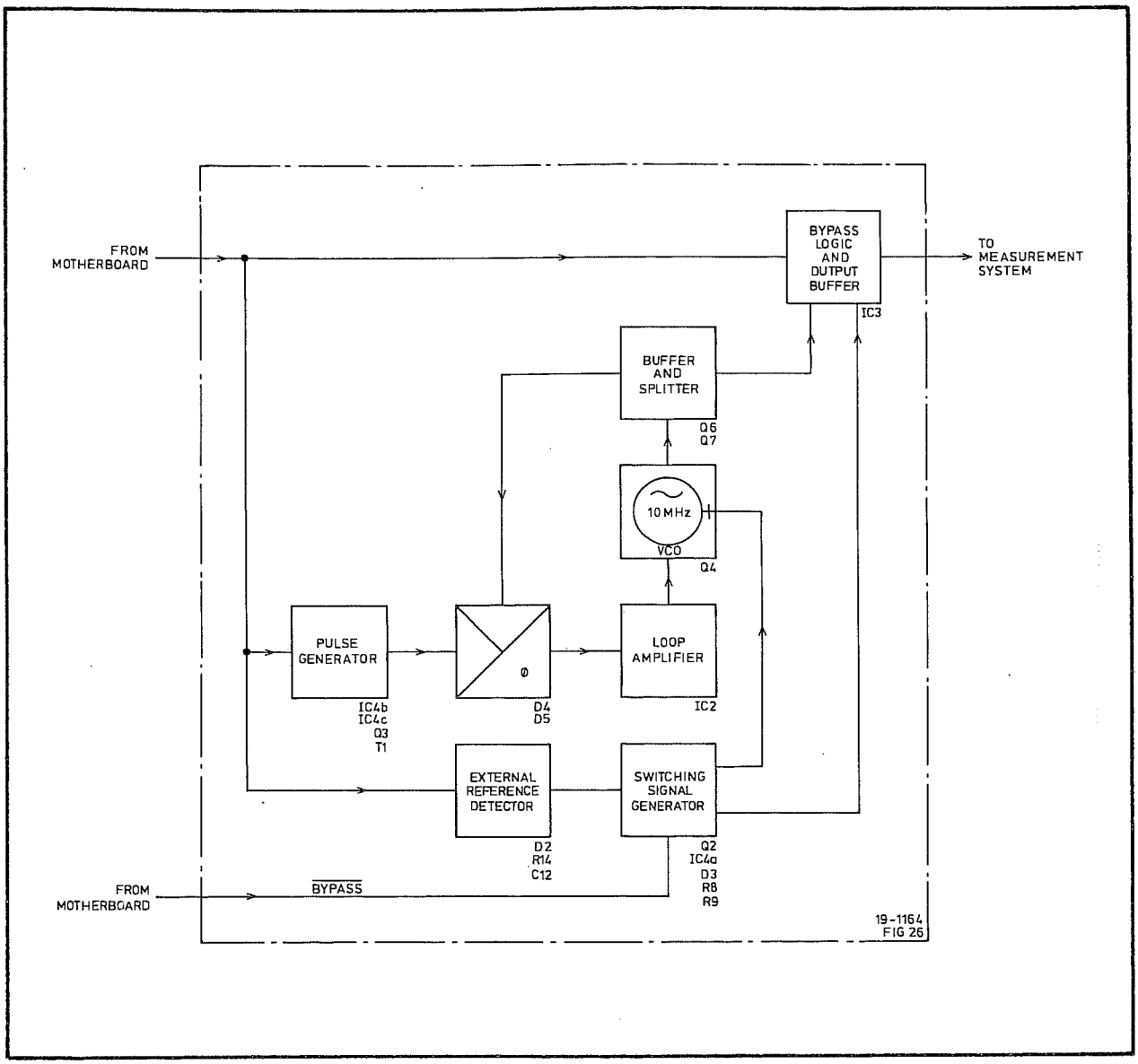


Fig. 6.17 The Reference Frequency Multiplier

Circuit Description

183 The circuit diagram is shown in Fig. 26 in Section 8.

Input Circuit and Pulse Generator

184 Two antiphase waveforms derived from the external reference signal enter the system at SK16 pins 6 and 9. The waveform at pin 9 is converted from ECL to TTL levels in Q1 and squared in IC4d before being applied to the pulse generator, IC4b and IC4c. The operation of this circuit is illustrated in Fig. 6.18.

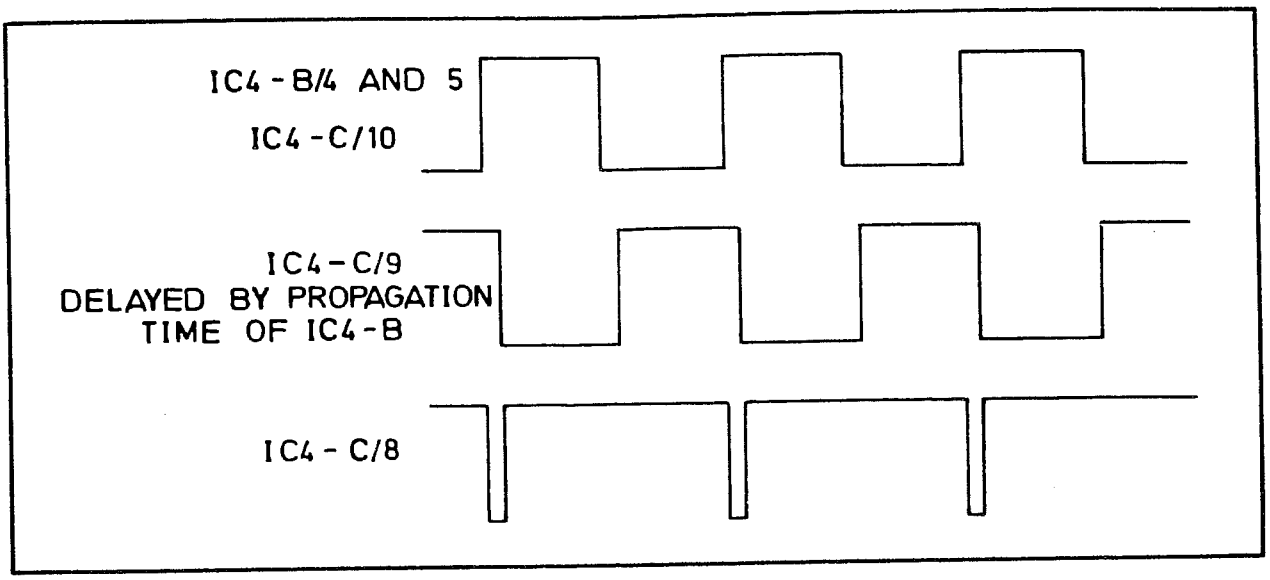


Fig. 6.18 Pulse Generator Waveforms

185 The negative-going pulses at IC4c/8 are used to switch Q3, which drives the transmission-line type transformer T1. The transformer acts as a phase splitter, so that for the duration of each pulse from IC4c/8, the sampling bridge of the phase detector is held forward biassed, with the D4A/D5A and D4B/D5B junctions symmetrical about 0 V.

The Phase-Locked Loop

186 The loop oscillator active element is Q4. The oscillator frequency is controlled by the crystal XL1 and the varactor diode D1. The trimming capacitor C2 can be adjusted to compensate for a range of crystal and varactor tolerances.

187 The oscillator output drives a unity-gain cascode buffer, Q6/Q7. The buffered signal from the collector of Q7 forms the RF input to the phase detector.

188 When the sampling bridge of the phase detector is forward biased by the pulses from T1, the D5A/D5B junction adopts the same potential as the D4A/D4B junction. At other times the junctions are isolated from each other by the high impedance of the non-conducting diodes. The bridge output is therefore a series of samples of the loop oscillator waveform, taken at the frequency of the external frequency standard.

189 The phase detector output depends upon the relative frequency of the loop oscillator and the frequency standard, and upon the phase of the loop oscillator waveform at the instant of sampling. If the standard frequency is 10 MHz every cycle of the loop oscillator output is sampled, but if it is a sub-multiple of 10 MHz only every second, fourth, fifth or tenth cycle will be sampled. In all cases, however, provided the standard frequency is an exact sub-multiple of the loop oscillator frequency, the samples will be of constant amplitude. If the standard frequency is not an exact sub-multiple of the loop oscillator frequency the output pulses will be amplitude modulated.

190 The amplitude of each phase detector output pulse depends upon the instantaneous value of the loop oscillator waveform at the instant of sampling. The pulses are integrated in C7 to form the input to the loop amplifier IC2. When the loop is in lock, the voltage across C7 maintains the voltage at IC2/6, and therefore across the varactor, at the level needed to maintain the loop oscillator at the lock frequency.

External Reference Detector and Bypass Switching

191 The output from IC4d/11 is fed to a detector formed by D2, C12 and R14. If no external reference signal is present at the EXT STD INPUT connector, SK16 pin 9 is held low, Q1 conducts and IC4d/11 is at logic '1'. The detector output, and therefore the base of Q2, is at +5 V and Q2 is switched off. A logic '0' level is applied to IC4a/2, giving a logic '1' at IC4a/3 and the base of Q5. The zener diode D3 converts the logic levels from TTL to the level required to switch Q5. R8 and R9 provide ECL logic levels for IC3b and c.

192 With Q5 switched on, the voltage across R4 holds the emitter of Q4 positive with respect to its base, disabling the oscillator. At the same time a logic '1' level taken from the junction of R8 and R9 is applied to IC3b/7 and IC3c/11. This disables IC3c and enables IC3a, so that the oscillator output line is open circuited and SK16 pin 6 is connected to SK16 pin 5 and 8 via IC3a and IC3d.

193 When an external reference signal is present at SK16 pin 9 the output from IC4d/11 is a TTL square wave at the external reference frequency. The detector output holds the base of Q2 negative, so that Q2 conducts and IC4a/2 is at logic '1'. Since IC4a/1 is held at logic '1' by +5 V at SK17 pin 4, IC4a/3 is at logic '0'. Under these conditions Q5 is cut off and the loop oscillator is enabled. A logic '0' is applied to IC3b/7 and IC3c/11 from the junction of R8 and R9. This disables IC3a and enables IC3c, so that the oscillator output is connected to SK16 pins 5 and 8 via IC3c and IC3d.

GPIB INTERFACE

Introduction

194 The GPIB Interface is a self-contained, microprocessor controlled system. It handles the transfer of data between its internal memory and the GPIB without involvement of the main instrument microprocessor. Data transfer is made one byte at a time, each transfer being controlled by the IEEE-488 handshake protocol. The circuit diagram is given in Fig. 9 in Section 8.

195 The microprocessor $\overline{\text{RESET}}$ signal is derived from the standby and IRQ system. The clock signal is derived from IC6, via Q22, shown in Fig.3 in Section 8.

196 The microprocessor uses a multiplexed bus, the eight low-order bits being used for both bus address and data. The low-order address bits are put onto the bus first, and are latched into IC11 by the address strobe. The bus is then free for data use.

197 Data transfer between the microprocessors is initiated by an interrupt, and is controlled by a three-wire handshake protocol. The transfer is in the form of a data string, the number of bytes in the string being indicated by the first byte.

Address Setting and Recognition

198 The microprocessor reads the settings of the address switches in Switchbank S1, via its port B inputs, approximately every 1 mS and writes the settings into an address register within the general purpose interface adapter (GPIA), IC12.

199 When the interface address is set on the bus by the controller, it is recognized by the GPIA by comparison with the contents of the internal address register.

Reading from the Bus

200 When the interface is addressed to listen, the GPIA conducts the handshake procedure up to the point where the ready for data (RFD) indication is given. At this point IC12/27 is at logic '0', giving a logic '1' level at IC18d/11. This puts three of the bilateral switches in IC13 to the conducting state, so completing the RFD line. The logic '0' at IC12/27 also puts the buffers in IC14 and IC15 to the receive condition. Data from the bus enters the GPIA data-in register, and IC12/40 goes to logic '0' to provide an interrupt request to the microprocessor, IC9.

201 The microprocessor interrupt routine establishes the reason for the interrupt. The address decoder, IC8, is enabled via IC6c, IC6d, IC7a, IC7b and IC7d, using address lines GA7, 9, 10, 11 and 12. The decoder is addressed using lines GA4, 5 and 6 and gives the GPIA enable signal at IC8/15. The data-in register of the GPIA is addressed using the R/W line and lines GA0, 1 and 2. The microprocessor then reads the contents of the data-in register and transfers the data to memory.

202 When the data-in register has been read, the GPIA cancels the interrupt request and allows the data accepted (DAC) line to go high. The handshake routine then continues, and a further byte, if available, is loaded into the data-in register. The interrupt and data transfer sequence is then repeated.

Writing to the Bus

203 When the GPIA is addressed to talk its internal data-out register will normally be empty. Under these conditions IC12/40 goes to logic '0' and provides an interrupt request to the microprocessor.

204 IC17a is in the reset state, giving a logic '1' at IC18d/12. Since IC12/27 is at logic '1' when the GPIA is addressed to talk, IC18d/13 is also at logic '1'. The resulting logic '0' at IC18d/11 open circuits three of the bilateral switches in IC13 to break the RFD line. The fourth bilateral switch conducts, due to the logic '1' at IC19c/10, and holds IC12/18 at 0 V. Even if the listening device asserts that it is ready for data, IC12 will not attempt to load the contents of the data-out register onto the bus.

205 The microprocessor interrupt routine establishes the reason for the interrupt. The microprocessor then enables the address decoder, IC8, via IC6c, IC6d, IC7a, IC7b and IC7c, using address lines GA7, 9, 10, 11 and 12. The decoder is addressed using lines GA4, 5 and 6, and gives the GPIA enable signal at IC8/15. The data-out register of the GPIA is addressed using the R/$\overline{W}$ line and lines GA0, 1 and 2, and a data byte is written into the register. The GPIA then cancels the interrupt request.

206 Following the data transfer, the microprocessor sets IC17a, using line PB7, to give a logic '0' at IC18d/12. This gives a logic '1' at IC18d/11, which enables three bilateral switches in IC13 and connects the RFD line. The fourth switch in IC13 is disabled, so releasing IC12/18 from 0 V. When the listening device asserts that it is ready for data, the GPIA loads the contents of the data-out register onto the bus and continues with the handshake routine.

207 When the data-out register has been read, the GPIA generates a further interrupt request. The microprocessor resets IC17a, using line PB6, giving a logic '1' at IC18d/12, so that the RFD line is again broken at IC13. The data transfer and data transmission sequence is then repeated.

Serial Poll

208 The status byte is only updated when the GPIA enters the serial poll active (SPAS) state. To do this, the two interface messages SPE and SPD are detected by IC6a and b, IC7d, IC18a and IC19b. These clock IC17a giving a logic '1' at IC18d/12, thereby, breaking the RFD line at IC13 and preventing the status byte handshake from taking place. The microprocessor now updates the status byte in the GPIA, presets IC17a giving a logic '0' at IC18d/12 which closes the switch in the RFD line allowing the handshake to be completed.

Data Transfer Between Microprocessors

209 Data transfer between microprocessors is made using the multiplexed data bus on both devices. Connection between the buses is made by means of a D-type latch, IC1 or IC2, depending on the direction of data transfer. All data transfers are initiated by the sending device. The first byte indicates the number of bytes to be transferred.

210 For data transfer to the GPIB microprocessor, the instrument microprocessor sets PL4 pin 22 (GPIB DATA IRQ) low. This provides an interrupt request (IRQ) to the GPIB microprocessor via IC4d. As part of the interrupt routine, IC8 is enabled and addressed to give an enabling signal for IC5d. The microprocessor reads the IRQ flag via IC5d and data bus line 7 to establish that the IRQ is from the instrument and not the GPIA.

211 The GPIB microprocessor prepares to receive data, and then enables and addresses IC8 to give a signal which clocks IC16a via IC20b. The level set on line 0 of the data bus is transferred to IC16/5, and forms the ready for data (RFD) signal to the instrument microprocessor.

212 The instrument microprocessor enables and addresses IC3 to give an enabling signal to IC5c, reads the RFD signal, puts the first data byte on the bus and readdresses IC3 to give a clock signal which latches the data into IC1. It then addresses IC3 to give a clock signal for IC16b, so that the logic level set at IC16b/12 is transferred to IC16b/9 to form the data valid (DAV) signal to the GPIB microprocessor.

213 The GPIB microprocessor addresses IC8 to give a signal to enable IC5a, and reads the DAV signal via data bus line 6. It then cancels its RFD signal, addresses IC8 to give an output signal for IC1 (via IC20c) and reads the data. A data accepted signal (DAC) is sent via IC2 and the RFD signal is reset. The instrument microprocessor responds by cancelling its DAV signal and entering the next data byte into IC1. Data transfer continues in this manner until the required number of bytes have been transferred.

214 Data transfer from the GPIB microprocessor to the instrument processor follows a similar pattern. The IRQ signal is passed from port A line 0 via IC18b and IC4c. The IRQ flag is read by the instrument microprocessor during its interrupt routine, via IC5b (enabled by an output from IC3). The IRQ signal is cancelled by the instrument microprocessor setting data bus line 0 to logic '0' and then addressing IC3 to clock IC17b. The resulting logic '0' at IC17b/9 disables IC18b.

215 During data transfer from the GPIB interface to the instrument, the RFD signal is passed via IC16b and IC5a, the DAV signal via IC16b and IC5c, the DAC signal via IC1 and the data via IC2.

BATTERY PACK (OPTION 07)

216 A block diagram of the battery pack option is shown in Fig. 6.19. The battery pack option allows the instrument to be supplied from a +12 V internal battery pack (part of this option) or from an external DC supply. The output from the option is only partially regulated. Fine regulation is done on the motherboard in the normal way.

217 The option is based on a switch-mode flyback converter. It includes a charging circuit for the internal batteries, a battery condition monitor, and other circuits to maintain the charge and optimize battery life.

Flyback Converter

218 This type of switch-mode DC-DC converter relies for its operation on switching a direct current repeatedly on and off, at high frequency, through the primary of a flyback transformer. The resultant AC from the secondaries is rectified to produce a range of DC levels. Output levels are controlled by feedback to the switching circuit.

219 In the block diagram of the option, shown in Fig. 6.19, direct current, from either the internal battery pack or an external DC supply, passes through the primary of the flyback transformer and through a transistor switch to ground.

220 Switching occurs at a frequency of approximately 40 kHz. Current is first switched on, allowing the magnetic field around the primary to build up. The current is then switched off and the collapsing field transfers its energy to the secondary windings. Secondary voltages are rectified and filtered to provide +15 VUR, +5 VUR and -5.2 VUR.

Feedback

221 For normal loads, the switching duty-cycle is such that the transformer core never has time to saturate, so the power transferred to the secondaries is proportional to the on-time of the transistor switch. In the pulse width modulator, the level of the +5 V output is compared with a reference voltage. If the +5 V is low, the on-time of the switch is increased, and if it is high, the on-time is reduced. Note that the switching frequency remains constant. Only the duty cycle is changed.

222 At higher load levels, the duty cycle is such that the secondary current does not have time to decay to zero between switching pulses. Therefore , the core still retains some energy at the end of the cycle. This means that the next on-time does not have to be increased to provide the extra power. Hence, beyond a certain load current, transistor on-time remains essentially constant. On-time will increase for a few cycles, however, at the instant the load current increases.

223 Feedback is taken from the +5 VUR rail because this has the heaviest load. Each of the other output levels is essentially governed by the ratio of its secondary turns to those of the +5 VUR secondary.

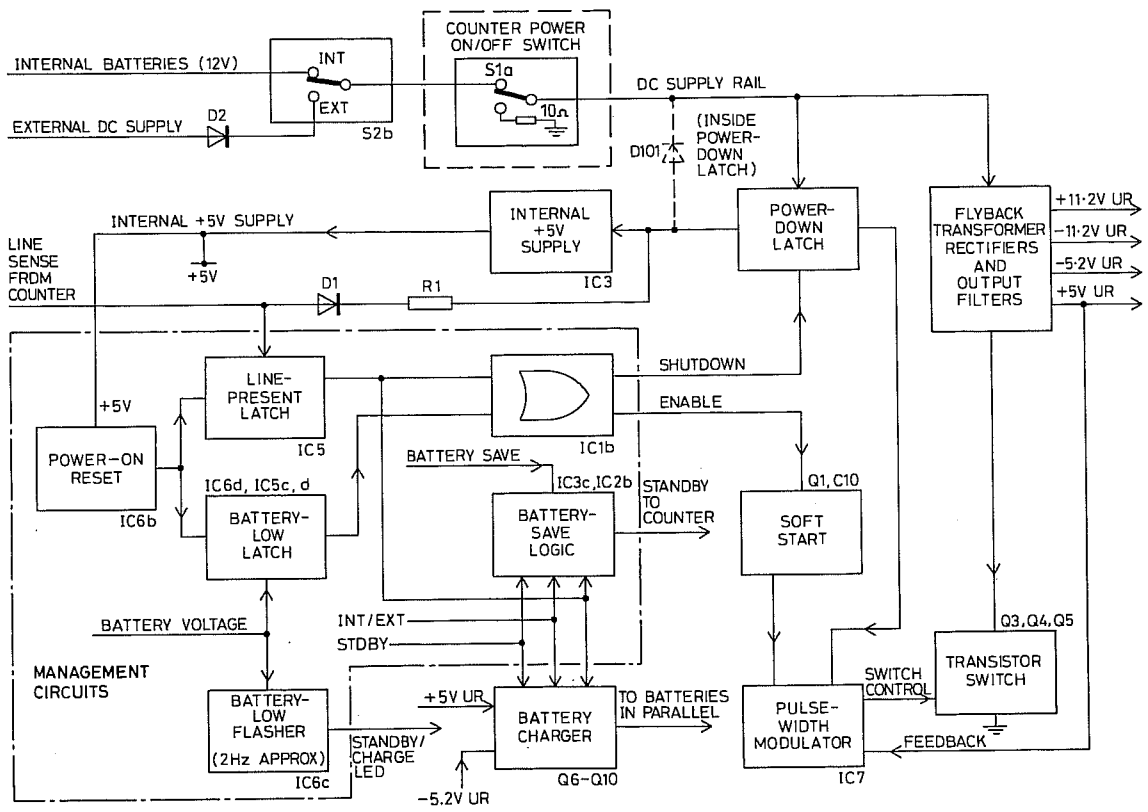


Fig. 6.19 The Battery Pack Option

Soft Start

224 At switch-on, the +5 V output would initially be zero. Therefore the feedback circuit just described would create a large current surge. To prevent this, soft start circuitry ensures that the Q5 on pulses are initially very short, and are only gradually increased to normal. Soft start is enabled by a signal from the management circuits.

Power-Down Latch

225 This is essentially an on/off switch for the pulse-width modulator and for a +5 V regulator. It is on when the instrument is being powered by the battery pack or an external DC supply. It is switched off when the battery is low (auto-shutdown), and when the instrument is being powered from an AC (line) supply.

Management Circuits

226 Control of the battery pack option, and its response to control switches and to variations in AC or DC supply levels is handled by the management circuits. These are identified in the block diagram.

Line Sense

227 When the instrument is being powered from line, an AC signal is available on the line sense input. This is used to operate the line present latch, which disables the pulse-width modulator via the power-down latch.

Battery Low/Auto-Shutdown

228 The battery voltage is monitored by the battery-low latch and the battery-low flasher. If the voltage falls to around +11 V the STBY/CHRG LED on the front panel is flashed at 2 Hz. After approximately 10 minutes further operation, when the voltage has dropped to around 10.1 V, the battery-low latch will be set and the option will be shut down by the power-down latch.

Battery-Save Facility

229 If the battery-save facility is selected, the battery-save logic will switch the instrument into standby mode on minute after it has been enabled.

Internal +5 V Supply

230 The control logic (management circuits) of the option need an independent +5 V supply. This is provided by a +5 V regulator.

231 When the instrument is using an AC supply, the regulator is powered by a DC voltage derived from the line sense input. When one of the DC inputs is being used, the regulator is supplied by the DC supply rail via the power-down latch.

Power-On Reset

232 When power is switched on, +5 V is applied to the power-on reset circuit. This circuit provides a pulse that resets the line-present and battery-low latches. If there is no AC input on line sense, the power-down latch will be cleared and the soft-start circuit enabled.

Battery Charging

233 The option includes a battery charger capable of fully-charging a battery pack within 14 hours, and a trickle charger designed to top- up a previously charged battery.

Battery Charger

234 This circuit can only be enabled when the instrument is powered from the line or from an external DC supply. The charger is powered from the +5 VUR and -5.2 VUR rails, and is enabled by the STDBY signal from the STBY/CHRG button.

235 The +12 V battery-pack is formed by two +6 V batteries connected in series. When the charger is enabled, an external relay configures the two batteries in parallel.

Trickle Charging

236 Whenever the instrument is powered from line, rectifier circuit D1/R1 derives a DC voltage from a 40 V peak-to-peak signal on the line sense input. This supplies approximately +14 V to the DC supply rail via D101 in the power-down latch. If the internal battery is selected, the DC supply rail provides a trickle-charge to top up the battery. Diode D102 prevents the external DC supply from being charged in this way.

Circuit Description

237 The circuit of the battery-pack assembly is shown in Fig. 17 in Section 8.

Power Sources

238 Option power can be supplied from line, from an external DC supply or from the battery pack.

239 When the instrument is powered by line, a 40 V peak-to-peak, 50 Hz signal is applied to LINE SENSE at SK21/15. This is rectified by D1 to give approximately 14 V DC. The voltage is fed via D101 (in the Switch Board Assembly) to the DC supply rail. In the absence of a line supply, the internal battery pack or an external DC supply can be selected at S2.

240 In the EXT position, a DC supply plugged into JK1 is connected via SK21/2-4, S1a (on the motherboard assembly 19-3022) and SK21/21-23, to the DC supply rail.

241 In the INT position of S2, the battery pack is connected to the DC supply rail by the same route.

Switching Circuit

242 Whenever IC7 is enabled, a nominal 40 kHz square wave signal at Pin 9 switches driver transistors Q3 and Q4 on and off in turn. (the totem- pole arrangement provides a fast switching action). This switches MOSFET Q5 on and off in time with the signal at IC7/9. The switching signal is derived from an internal oscillator, the frequency of which is controlled by the value of C13.

Flyback Transformer

243 When Q5 is ON, a primary current flows and energy is built up in the core. Under these conditions the voltages developed across the secondaries reverse bias the rectifier diodes D7, D9 and D10. When Q5 is switched OFF, the field generated by the primary winding collapses, reversing the secondary voltages and forward biasing D7, D9 and D10. This releases the energy stored in the core, to the load via the rectifier diodes.

244 C16, C18 and C19 filter the outputs from the rectifiers to produce the +15 VUR, +5 VUR and -5.2 VUR rails.

Level Control

245 A voltage proportional to the +5 VUR level is developed across R30 and sensed by the ERROR input (IC7/7) of the pulse-width modulator. IC7 compares this error signal with the level of an internally generated reference voltage. This controls the duty cycle of the switching signal at IC7/9, which reduces the error on the +5 V UR line.

246 R28 modifies the feedback level, allowing the controlled level to be set precisely.

Soft Start Circuit

247 R26 and C11 form a feedback-loop stability network for the circuit within IC7 that compares reference and feedback levels. Shunting these components has the same effect as a decrease in the +5 VUR level. This effect is used to produce a soft start at switch-on. The sequence is as follows.

248 When the switch-mode circuits are not operating, a high on IC1b/13 disables IC7 via the power-down latch, and maintains Q1 in the conducting state, holding the base of Q2 close to 0 V, pulling it's emitter down to nominally +0.7 V, shunting C11 and R26.

249 When IC1b/13 goes low, IC7 is enabled and Q1 is switched off allowing C10 to charge via R24.

250 As the base voltage of Q2 slowly rises so will it's emitter, allowing the output rails to only slowly increase. Eventually Q2 base voltage rises above the normal voltage range on IC7/8, Q2 base/emitter then becomes reverse biased, and the clamping effect of Q2 is removed and the pulse-width modulator operates normally.

Power-Down Latch

251 When there is no line supply, the +5 V regulator for the management circuits is powered by the DC supply rail, via the power-down latch. A power-up circuit formed by Q103, R108, R109 and C102, ensures that the latch is on at power-up. Once the management circuits are enabled, the latch condition will depend upon the logic signals generated by the management circuits.

252 At power-up, the base of Q103 is held low, switching on Q103 while C102 charges. The voltage developed across R107, switches on Q101, which in turn switches on Q102, Q104 and Q105.

253 Q102 latches Q101 on by maintaining current through R107 and R104. Thus the circuit remains latched on when C102 is charged and Q103 switched off.

254 Q105 connects the DC supply rail to Vcc on IC7.

255 Q104 connects the DC supply rail to the +5 V regulator IC8, thereby energizing the management circuits.

256 Unless the line supply is on, or the DC supply rail is low, the latch will remain on. However, if one of those conditions exists, a high on IC1b/13 will drive the base of Q101 low, thus breaking the connection between the DC supply rail, and IC7 and IC8. In this state the current drain on the DC supply rail will be almost nil.

Trickle-Charge Circuit

257 The 40 V peak-to-peak line sense signal is rectified by D1/R1. This provides approximately +14 V DC to supply the +5 V regulator, and to trickle-charge the battery-pack (via D101 in the power-down latch).

Full Charge Circuit

258 The charger is of the current-limited constant voltage type. The charger circuit is powered by the +5 VUR and -5.2 VUR rails. When the instrument is using the line supply, the two rails are supplied from circuits on the motherboard, otherwise they are supplied from the switch-mode circuits.

259 It is only possible to enable the charger when a line supply or an external DC supply is being used. When the internal +12 V supply is selected the charger is disabled by a ground on S2a.

260 The charger is enabled when STBY goes high, generating a high on IC3d/11. This switches on Q6 and the constant current circuit formed by D11, Q7, R34 and RL1.

261 RL1-a to RL1-d connect the two 6 V batteries, in parallel, between the -5.2 VUR rail and the cathode of D15.

262 To provide temperature stability, it is necessary to make the charger voltage vary with temperature at a rate of approximately -8 mV/°C. This is done by using the base-emitter junction of Q8 (-2 mV/°C) as a temperature sensor, and then multiplying the sensor voltage by four.

263 The circuit comprising Q8, IC4a, R40, Q9, Q10, D15, R41 and R38 performs the multiplication. IC4a adds the result to a reference voltage from the wiper of R36, which provides adjustment of the charger output voltage, set at +7.63 V at 23°C.

264 A stable voltage for the reference divider chain R36, R37 and R45 is provided by D13 and R35.

265 Charge current passes through R1, Q10 and D15 to the two batteries connected in parallel. The voltage across R1 is sampled by R43 and R44, and is compared against a fixed voltage reference by IC4b. The output of IC4b controls the non-inverting input of IC4a, via D14, to limit the maximum current drawn by the batteries. While the charge current remains below this preset maximum limit, the output from IC4b always reverse biases D14, therefore, the operation of the charge- voltage control loop is not affected.

266 D15 prevents the batteries being discharged due to fault conditions in the charging circuit.

Line Sense Circuit

267 The presence of the 40 V peak-to-peak signal is detected by R8, R9, D5, D6, IC5a and IC5b.

268 R8 and R9 attenuate the signal, D5 and D6 limit it to +5 V and 0 V.

269 IC5a and IC5b form the line present latch, which is set by the first rising edge on IC5b/6, thus providing a high on IC1b/12 and IC3a/1. The line present latch will remain set until the unit is switched off.

Battery Low Indication and Auto-Shutdown

270 Battery voltage is monitored by IC6c via potential divider R10-R13. If the battery drops below approximately 11 V, IC6c will turn on the oscillator formed by IC3b and IC2d. The output of this oscillator (which is high when disabled) is then Exclusive ORed with the STDBY signal and its output used to flash the STBY/CHRG LED at approximately 2 Hz.

271 If the battery falls to below approximately 10.1 V, the output of IC6d (Battery-Down comparator) goes high and sets the battery-low latch (IC5c and d), giving a logic '1' at IC5c/10. This trips the power-down latch into the off state via IC1b and IC6a, shutting down the converter and reducing battery drain to nil.

NOTE: With the internal battery selected, the battery-low indicator will start flashing approximately 10 minutes before the power- down latch disables the unit.

Power-On Reset Circuit

272 At power-up, the non-inverting input of IC6b rises to approximately 3.3 V. The inverting input, however, is held lower as C6 charges.

273 While its inverting input is low, IC6b/1 is high, clearing the battery-low and line present latches. Once C6 is charged, IC6b/1 will change state, allowing the latches to be controlled by the line- present and battery-low voltages.

Standby/Battery-Save Operation

274 Successive depressions of the STBY/CHRG button operate a bistable circuit on the motherboard. In the set state this puts the instrument in the standby mode and asserts STDBY at SK21 pin 16. In the clear state, the instrument is put into normal operation mode and the STDBY line is at logic '0'. Control of the bistable circuit, and the effect of the STDBY signal, is modified by the NORMAL/BATTERY SAVE and the EXTERNAL/INTERNAL switches.

275 When powered from an AC line (IC3a/1 high) or an external battery (IC3a/2 high), the STBY/CHRG button enables and disables the charger as previously described. When STDBY is high, SK21 pin 7 is low. This drives the STBY LED, which in this event is used as a charging indicator. NOT STBY TRIG is disabled at IC1a/2.

276 When powered by the internal battery, both inputs to IC3a are low. This disables the charger and removes the disable from IC1a/2. The STBY/CHRG button is used to enable and disable the standby mode and the STBY LED is used as a standby indicator. The standby function is modified by the state of the NORMAL/BATTERY SAVE switch as follows:

(1) When S1 is in the NORMAL position, NOT 'STBY TRIG' is disabled at IC1a/5. If STDBY is asserted the unit goes to standby mode and the STBY LED comes on. If STDBY is negated, the unit reverts to normal operating mode and the STBY LED goes off.

(2) When S1 is switched to the BATTERY SAVE position, IC3c/9 and IC1a/5 are set to low by BATT SAVE TRIG active low, activated by IC18 on the motherboard. If STBY is in its high state, these changes will have no effect. However, if STBY is low or is subsequently toggled to its low state, IC1a/3 will go low and IC3c/10 will go high.

(3) C2 transfers this high to IC2b/5, causing a high on IC2b/4. This has no effect on IC1a/4, which is clamped to +5 V by D3.

(4) As C2 charges, the current through R6 will fall exponentially until, after approximately 1 minute, IC2b/5 will fall below the threshold level, taking IC1a/4 low.

(5) With all its inputs low, IC1a asserts STBY TRIG active low, which toggles the standby bistable on the main unit (hence the STDBY signal), putting the instrument into standby mode and lighting the STBY LED.

(6) Subsequent operation of the STBY/CHRG button will put the instrument into the normal operating mode and initiate another one-minute cycle.

SECTION 7 MAINTENANCE

INTRODUCTION

1 This section is in six parts, which relate to:

(1) Test equipment required.

(2) Dismantling and reassembly.

(3) Special functions for diagnostic purposes.

(4) Fault finding.

(5) Setting up instructions for use after repair, or if the instrument fails the overall performance verification.

(6) Overall performance verification procedure (PVP).

TEST EQUIPMENT REQUIRED

2 A complete list of test equipment required to carry out the procedures described in this section is given in TABLE 7.1. The items required for each operation are listed at the start of the relevant instructions.

3 A particular model of test equipment is recommended in some cases, but other equipment having the required parameters given in TABLE 7.1 may be used. Although the procedures to be followed are given in general terms, they are based on the use of the recommended test equipment. Some modification to the procedure may be necessary if other test equipment is used.

TABLE 7.1

Test Equipment Required

Item	Description of Recommended Model	Required Parameters
1	Synthesized Signal Source, Gigatronics 905/0.05-26.	0.5 - 20 GHz, low phase noise. 10 MHz Internal Reference output. -34 dBm to -29 dBm.
2	Synthesized Signal Generator, Racal Dana 3101 with Option 02.	100 kHz to 1.3 GHz, low phase noise. 10 MHz Internal Reference output. -1 dBm to -57 dBm.
3 (i)	Synthesized Audio Source, Hewlett Packard 3325B with Option 001.	10 Hz to 5 kHz. 10 MHz Internal Reference output 18 mV RMS.
4	Power Meter, HP436A with HP8482A sensor.	40 MHz to 1.3 GHz. -30 dBm to -3 dBm.
5	Power Meter, HP436A with HP8485A sensor.	0.5 GHz to 20 GHz. -16 dBm to -9 dBm.
6 (ii)	Digital Multimeter (2 Off) Racal Dana 4008.	DC voltage to 20 V. DC current 10 uA to 2 A. Test voltage for resistance measurements to be <0.5 V.
7	Oscilloscope, Racal Dana 4023.	100 MHz bandwidth, Y input sensitivity 10 mV/division.
8	Probe. The probe included with the Racal Dana 4023 is suitable (item 7).	x1/x10 combination probe for use with the DMM and the oscilloscope.
9	Frequency Standard, Racal Dana 9475.	10 MHz, +/-3 parts in 10^{10}.
10	GPIB Controller, HP85.	
11	GPIB Analyzer, Tero-Test.	
12 (iii)	DC Power Supply, Racal Dana 9232.	0 V to 16 V minimum at 2 A.

TABLE 7.1 (Continued)

Test Equipment Required

Item	Description of Recommended Model	Required Parameters
13	Precision Power Splitter, HP11667B.	50 Ohms; 2 resistor; PC3.5(f); 0.5 GHz to 20 GHz; Tracking:- ≤0.25 dB to 18 GHz, ≤0.4 dB beyond.
14	Precision Attenuator, HP8493C, Option 020.	20 dB, 50 Ohms, PC3.5(m) -PC3.5(f), 290 MHz to 20 GHz. Accuracy better than +/-0.5 dB up to 18 GHz, +/-0.6 dB beyond.
15	Feed-through Termination, Suhner 6701.01.A	50 Ohms, BNC(m)-BNC(f).
16	Coaxial Lead (2 off).	SMC(f)-SMC(f), 1 m long.
17	Coaxial Lead, Suhner: SUCOFLEX 103/100cm/11PC3.5/11PC3.5/ 0.5-26.5GHz.	PC3.5(m)-PC3.5(m), 1 m long. Insertion loss <2 dB, 0.5 GHz to 20 GHz.
18	Coaxial Lead (2 off).	BNC(m)-BNC(m), 1 m long.
19	Coaxial Adaptor, Suhner 32 N-SMC-50-1.	N(m)-SMC(m).
20	Coaxial Adaptor, Suhner 33 SMC-N-50-1.	N(f)-SMC(m).
21	Coaxial Adaptor, Suhner 32 N-SMA-50-51.	Precision N(m)-SMA(m).
22	Coaxial Adaptor, Suhner 31 BNC-SMA-50-1.	BNC(f)-SMA(f).
23	Coaxial Adaptor, Suhner 32 BNC-SMC-50-2.	BNC(m)-SMC(m).
24	Coaxial Adaptor, Suhner 33 N-BNC-50-1.	N(m)-BNC(f).
25	Coaxial Adaptor, Suhner 31 BNC-N-50-1.	N(f)-BNC(f).
26 (iv)	Coaxial Adaptor, Suhner 33 N-SMA-50-51.	Precision N(m)-SMA(f).

TABLE 7.1 (Continued)

Test Equipment Required

Item	Description of Recommended Model	Required Parameters
27 (iii)	External DC Input Lead.	Red and black leads, 2.1 mm coaxial power jack to open-ends, 1 m long. Red lead to centre conductor of the coaxial connector.
28	Connecting Lead, Racal Dana 10-3274.	Extended ribbon cable for LO Synthesizer assembly.
29	Connecting Lead, Racal Dana 10-3273.	Extended ribbon cable for IF Synthesizer assembly.
30	Connecting Lead, Racal Dana 10-3267.	Ribbon extender cable for use when servicing the Battery Pack option.
31	Ring Nut Driver, Racal Dana 14-3013.	Combination ring nut driver to suit both types of ring nut used on the 2101.
32	Trimming Tool, Radio Spares 662-692, (Set of seven types).	Tip Dimensions: 2.3mm L max x 0.5mm W max x 0.6mm D min. Shaft, excluding handle, must be at least 20 mm long and <4 mm in diameter.
33	Adaptor, Radio Spares 456-009.	BNC(f)-4mm Plug Adaptor.
34 (i)	Non-synthesized Audio Source, Racal Dana 9083.	10 Hz to 5 kHz, 25 mV RMS.
35 (v)	Coaxial Adaptor, Suhner 32 PC3.5-50-0-1.	PC3.5(m)-PC3.5(m).
36	DC Block type N, Lucas Weinschel 7003	Min. frequency range 500 kHz to 200 MHz.
37	Torque Wrench, Suhner 74Z-0-0-21	For tightening SMA/PC3.5 connectors.
38	Torque Wrench Suhner 74Z-0-0-45	For tightening SMC connectors.

Notes Referring to TABLE 7.1

(i) Only one required, see INPUT A AF Sensitivity PVP.

(ii) Only one of item 6 required if no Battery Pack option fitted.

(iii) Required only for the Battery Pack option.

(iv) Not required if Rear Inputs Option 01 is fitted.

(v) Only required if Rear Inputs Option 01 is fitted.

DISMANTLING AND REASSEMBLY

Introduction

4 Instructions for dismantling and reassembling the 2101 are limited to those areas where special care is needed or difficulty may be experienced.

WARNING: LETHAL VOLTAGES
DANGEROUS AC VOLTAGES ARE EXPOSED WHEN THE EQUIPMENT IS CONNECTED TO THE AC SUPPLY WITH THE COVERS REMOVED. SWITCH THE INSTRUMENT OFF AND DISCONNECT THE SUPPLY SOCKET FROM THE REAR PANEL BEFORE CARRYING OUT ANY DISMANTLING OR REASSEMBLY OPERATION.

Instrument Covers

5 (1) Disconnect the power input socket from the rear panel.

(2) Remove the two screws securing the rear panel bezel: remove the bezel.

(3) Remove the two bungs located on each side and towards the front of the instrument.

NOTE: If the handles are fitted, peel off the adhesive trim patch from both handles. Remove the two screws securing each handle, remove the handles and spacers.

(4) Remove the top cover by sliding it to the rear of the instrument.

(5) Remove the bottom cover by sliding it to the rear of the instrument.

6 To replace the covers, follow the reverse of the previous procedure. Ensure that the top cover is fitted with the access holes towards the front of the instrument, and that the tongues on the ends of the covers are fitted under the edges of the front panel and rear bezel.

Front Panel

7 (1) Remove the instrument covers.

(2) Remove the ring nuts from the Input A and Input C connectors using the ring nut driver type 14-3013.

(3) Remove the Module Stack as described in the section under that title.

(4) Remove the Sampler Module as described in the section under that title.

(5) Remove the two screws securing the front panel to the side frame at both sides of the instrument.

(6) Remove the right-angled SMB connector from the rear of Input B adaptor.

(7) Carefully ease the front panel forward until the display board disconnects from the motherboard at PL1 and PL2.

8 To replace the panel, follow the reverse procedure. Pass the POWER switch button through the aperture in the panel and reconnect the SMB connector to the rear of Input B adaptor before securing the panel.

Rear Panel

9 (1) Remove the instrument covers.

(2) Remove the GPIB as described in the section under that title.

(3) If an ovened frequency standard (Option 04A or 04B) is fitted, remove the screws securing it to the rear panel. Pull the standard upwards until the board disconnects from the motherboard at PL14. If the PXO or TCXO is fitted, remove the screws securing it to the rear panel. This item does not have to be removed from the instrument.

(4) Remove the two screws securing the rear panel to the side frame at both sides of the instrument.

(5) Remove the nut from the I.F. Output connector.

(6) Remove the M3 nut and washer securing the rear panel to the AC input assembly.

(7) Ease the rear panel away from the instrument until it disconnects from the motherboard at PL19 and PL20.

10 To replace the panel, follow the reverse procedure.

Input B Prescaler Assembly

11 (1) Remove the instrument covers and the GPIB.

(2) Remove the Module Stack and the Sampler Module assembly.

(3) Remove the SMB connector from the rear of Input B adaptor.

(4) Remove the two screws securing the prescaler to the sideframe.

(5) Tilt the top of the prescaler slightly to clear the GPIB mounting. Carefully lift the prescaler vertically so that it disconnects from PL7.

12 To replace the prescaler, follow the reverse procedure.

Display Board

13 (1) Remove the instrument covers and the front panel as previously described.

(2) Remove the three screws securing the display board to the front panel.

(3) Turn the complete assembly over so that the display board is underneath.

(4) Lift the front panel away from the display board.

14 To replace the board, follow the reverse procedure.

Module Stack

15 (1) Remove two screws securing the module stack to each side of the instrument frame.

(2) Disconnect the ribbon cables from the module stack.

(3) Carefully lift the module stack part way out of the instrument and remove the coaxial cables at PL6, PL8, PL33 and PL39.

(4) Lift the module stack completely out of the instrument.

(5) To remove the IF Processor or LO Module from the module stack, remove the screws securing the relevant module and remove that module.

16 To replace the module stack, follow the reverse procedure.

NOTE: (1) All cables must be replaced as shown in the layout diagram label located on the inside of the instruments top cover.

(2) Torque all SMC connectors to 0.35 Nm using the SMC torque wrench.

LO Module

17 Before dismantling the LO Module, remove it from the Module Stack. See the section entitled 'Module Stack'. To dismantle the module proceed as follows:

(1) Remove the four M3 screws securing the lid to the module case. Lift the lid and the sealing gasket from the module, exposing the PCB.

NOTE: Before removing the lid make a note of the orientation of the lid. The lid must be replaced in the same orientation during reassembly.

(2) Remove the two sets of nuts and washers securing the PCB connector to the front of the module case.

(3) Remove the two M2.5 screws securing the PCB connector to the base of the module. Remove the two sets of screws and washers securing the rear of the PCB to the base of the module case. Lift the PCB vertically out of the module case.

18 To reassemble the module, follow the reverse procedure.

IF Module

19 Before dismantling the IF Module, remove it from the Module Stack. See the section entitled 'Module Stack'. To dismantle the module proceed as follows:

(1) Remove the four M3 screws securing the lid to the module case. Lift the lid and the sealing gasket from the module, exposing the PCB.

NOTE: Before removing the lid make a note of the orientation of the lid. The lid must be replaced in the same orientation during reassembly.

(2) Remove the two sets of nuts and washers securing the PCB connector to the front of the module case.

(3) Remove the two M2.5 screws securing the PCB connector to the base of the module. Remove the two sets of screws and washers securing the rear of the PCB to the base of the module case. Lift the PCB vertically out of the module case.

20 To reassemble the module, follow the reverse procedure.

Sampler/Power Limiter (OPT 11) Assembly

21 (1) Remove the instrument covers and the module stack.

(2) Remove the screw securing the sampler bracket to the instrument side frame.

(3) Remove the ring nut from Input C connector.

(4) Disconnect SK15 from PL15 on the motherboard.

(5) Disconnect PL32 and PL36 from the sampler.

(6) Lift the complete sampler bracket assembly out of the instrument ensuring that the rear of the assembly is clear of obstructions on the motherboard.

Removing the Sampler Module 17-1102 (Units WITHOUT OPT 11)

22 Refer to Fig. 7.1 when removing the module. Proceed as follows:

(1) Loosen the two screws 'c' securing the Sampler to the bracket.

(2) Disconnect the SMA connector 'b' from the Sampler Module.

(3) Remove the Sampler securing screws and lift the module clear of the bracket.

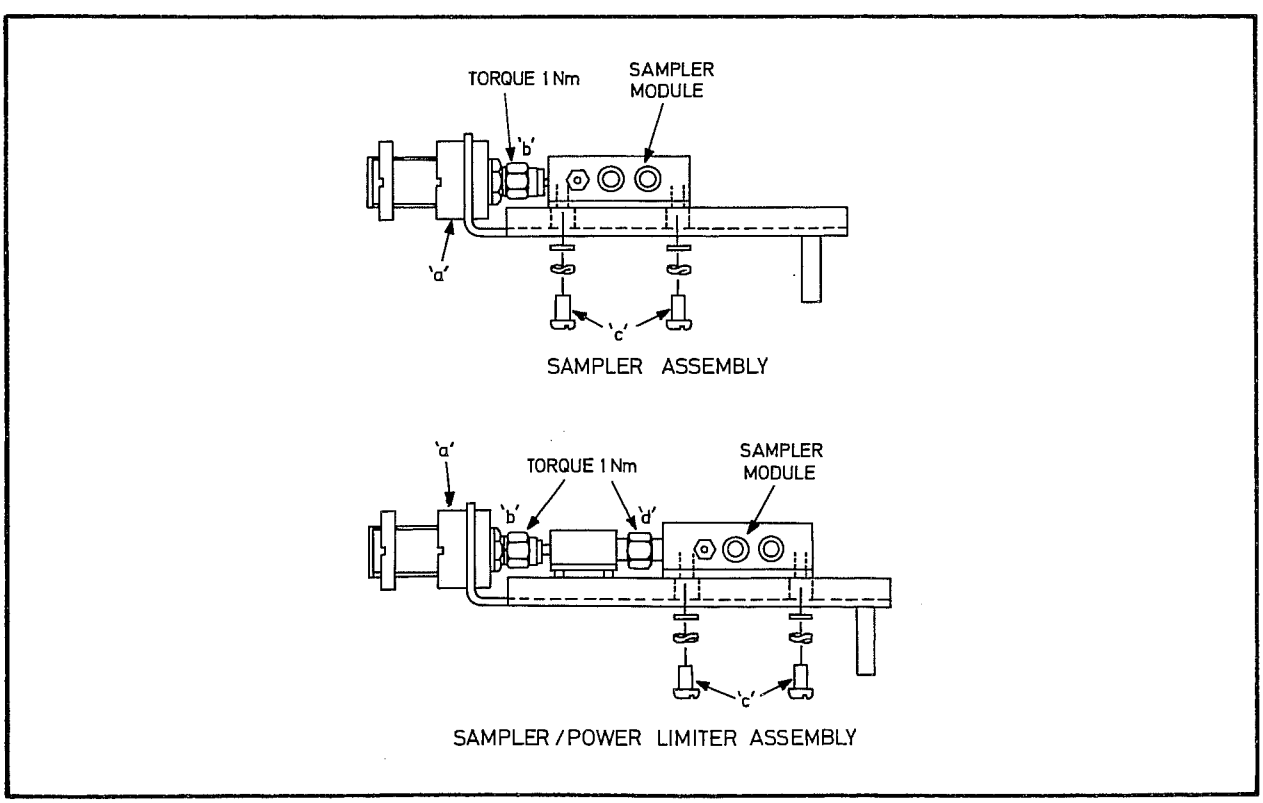


Fig. 7.1 Sampler and Sampler/Power Limiter (OPT 11) Assemblies

Replacing the Sampler Module 17-1102 (Units WITHOUT OPT 11)

23 Refer to Fig. 7.1 when replacing the module. Proceed as follows:

(1) Loosen Input C connector ring nut 'a', then retighten finger- tight.

(2) Connect Sampler Module 17-1102 to connector 'b' finger-tight only.

(3) Fit the Sampler securing screws 'c' finger-tight only.

(4) Tighten connector 'b' to 1 Nm using the SMA torque wrench.

(5) Fully tighten Input C connector ring nut.

(6) Fully tighten the Sampler securing screws 'c'.

Removing the Sampler Module 17-1102 (Units WITH OPT 11)

24 Refer to Fig. 7.1 when removing the module. Proceed as follows:

(1) Loosen the two screws 'c' securing the Sampler to the bracket.

(2) Disconnect the SMA connector 'd' from the Sampler Module.

(3) Remove the Sampler securing screws and lift the module clear of the bracket.

Replacing the Sampler Module 17-1102 (Units WITH OPT 11)

25 Refer to Fig. 7.1 when replacing the module. Proceed as follows:

(1) Loosen Input C connector ring nut 'a', then retighten finger- tight.

(2) Connect Sampler Module 17-1102 to connector 'd' finger-tight only.

(3) Fit the Sampler securing screws 'c' finger-tight only.

(4) Tighten connector 'd' to 1 Nm using the SMA torque wrench.

(5) Fully tighten Input C connector ring nut 'a'.

(6) Fully tighten the Sampler securing screws 'c'.

Removing the Power Limiter Option (OPT 11)

26 Refer to Fig. 7.1 when removing the module. Proceed as follows:

(1) Remove the Sampler Module as previously described.

(2) Disconnect the SMA connector 'b' and remove the Power Limiter Module.

Replacing the Power Limiter Option (OPT 11)

27 Refer to Fig. 7.1 when replacing the module. Proceed as follows:

(1) Loosen Input C connector ring nut 'a', then retighten finger- tight.

(2) Connect the Power Limiter Module to connector 'b' and tighten the connector finger-tight only.

(3) Connect the Sampler Module to connector 'd' and tighten the connector finger-tight only.

(4) Fit the Sampler securing screws 'c' and tighten finger-tight only.

(5) Tighten connector 'b' to 1 Nm ensuring that the Power Limiter Module does not rotate.

(6) Tighten connector 'd' to 1 Nm ensuring that the Power Limiter Module does not rotate.

(7) Tighten Channel C ring nut 'a'.

(8) Tighten the Sampler Module securing screws 'c'.

Removal of the GPIB

28 If the Battery Pack Option is to be fitted to the instrument, the GPIB must first be removed. To remove the GPIB proceed as follows:

(1) Disconnect the AC power cord at the rear panel.

(2) Remove the instrument covers.

(3) Remove the two M3 screws and toothed washers that secure the GPIB connector bracket to the instrument rear panel. Retain the screws and washers.

(4) Remove the two self-tapping screws that secure the GPIB board. Retain the screws.

(5) Disconnect the GPIB ribbon cable from SK4.

(6) Tilt the GPIB board upwards at the forward edge and lift it forwards clear of the instrument.

(7) Remove the two GPIB securing brackets on the side frames of the instrument.

Refitting the GPIB

29 To refit the GPIB proceed as follows:

(1) Hold the GPIB board, component side down, with the GPIB connector towards the rear panel. Connect the ribbon-cable to the motherboard at SK4.

(2) Tilt the GPIB board, and lower it into the instrument, easing the GPIB connector into the shaped cut-out in the rear panel of the instrument.

(3) Line up the holes in the GPIB board with the speednuts (move the speednuts slightly if necessary). Insert the two self- tapping screws through the board into the speednuts. Do not tighten the screws.

(4) Secure the bracket which carries the GPIB connector to the rear panel, using the two M3 screws and shakeproof washers. Tighten the screws.

NOTE: The screws and toothed washers provide the ground connection between the GPIB connector and the instrument chassis. Tighten the screws firmly to ensure that a good connection is obtained.

(5) Tighten the screws in (3).

(6) Replace the top cover. Replace and secure the bezel.

Rear Inputs (OPT 01) Assembly

30 To dismantle the Rear Inputs Assembly, if fitted, proceed as follows:

(1) Remove the instrument covers and the GPIB, or if fitted, the Battery Pack Option.

NOTE: Note the positions, routes and connections of the cables to the Assembly before dismantling it.

(2) Remove the two M3 screws and crinkle washers securing the assembly to the rear panel.

(3) If necessary, remove the frequency standard module.

(4) To remove the Sampler Module 17-1102, proceed as follows:

(a) Remove the two Sampler securing screws (M3x4 CSK. TAPTITE).

(b) Disconnect the two SMC coaxes from the Sampler, noting their position.

(c) Unsolder the two-wire cable from the Sampler, noting the terminal to which each wire is connected.

31 To reassemble the Rear Inputs Assembly, follow the reverse of the previous procedure. Ensure that the cables are reconnected and routed correctly.

SPECIAL FUNCTIONS FOR DIAGNOSTIC/CALIBRATION PURPOSES

32 The special functions listed in Table 7.2 are provided for use during maintenance. The functions are used in conjunction with the CHECK mode. They are entered in the special function register by pressing:

N N SHIFT STORE SF

where N N is the special function number, and enabled by pressing:

SHIFT SF

TABLE 7.2

Additional Special Functions

Function Number	Function with CHECK Mode Selected
70	10 MHz check
71	LED check
72	Measurement of short start TEC count
73	Measurement of long start TEC count
74	Measurement of short stop TEC count
75	Measurement of long stop TEC count

Special Function 70

33 Special function 70 is the default state of the 70 series special functions. It provides measurement of the 10 MHz internal frequency standard, and verifies operation of the microprocessor, MCC1, MCC2 and the TEC.

Special Function 71

34 Special function 71 exercises all the LEDs, except STANDBY, GATE, REM, ADDRESS and SRQ, at approximately 0.1 Hz. If the GPIB interface is fitted, the REM, ADDR and SRQ indicators light.

Special Functions 72, 73, 74 and 75

35 Special functions 72, 73, 74 and 75 should only be used for diagnostic purposes at an ambient temperature of 23°C +/-2°C.

36 The long counts must be 800 +/-220. The short counts must be in the range (0.5 x long count) +20/-40. Counts outside these ranges indicate that the TEC has failed.

FAULT FINDING

37 A guide to fault location is given in the flow charts of Fig. 7.2a to Fig. 7.2i. The charts provide a logical procedure for localizing the fault to an area of the circuit. When using the charts it is essential to begin at the start point in Fig. 7.2a and act accordingly to the results of each decision box met in turn. Starting part way through any chart is unlikely to lead to satisfactory fault location.

38 Test equipment required:

Item	Table 7.1 Item No
Digital Multimeter	6
Oscilloscope	7
Probe	8
GPIB Controller	10
GPIB Analyzer	11

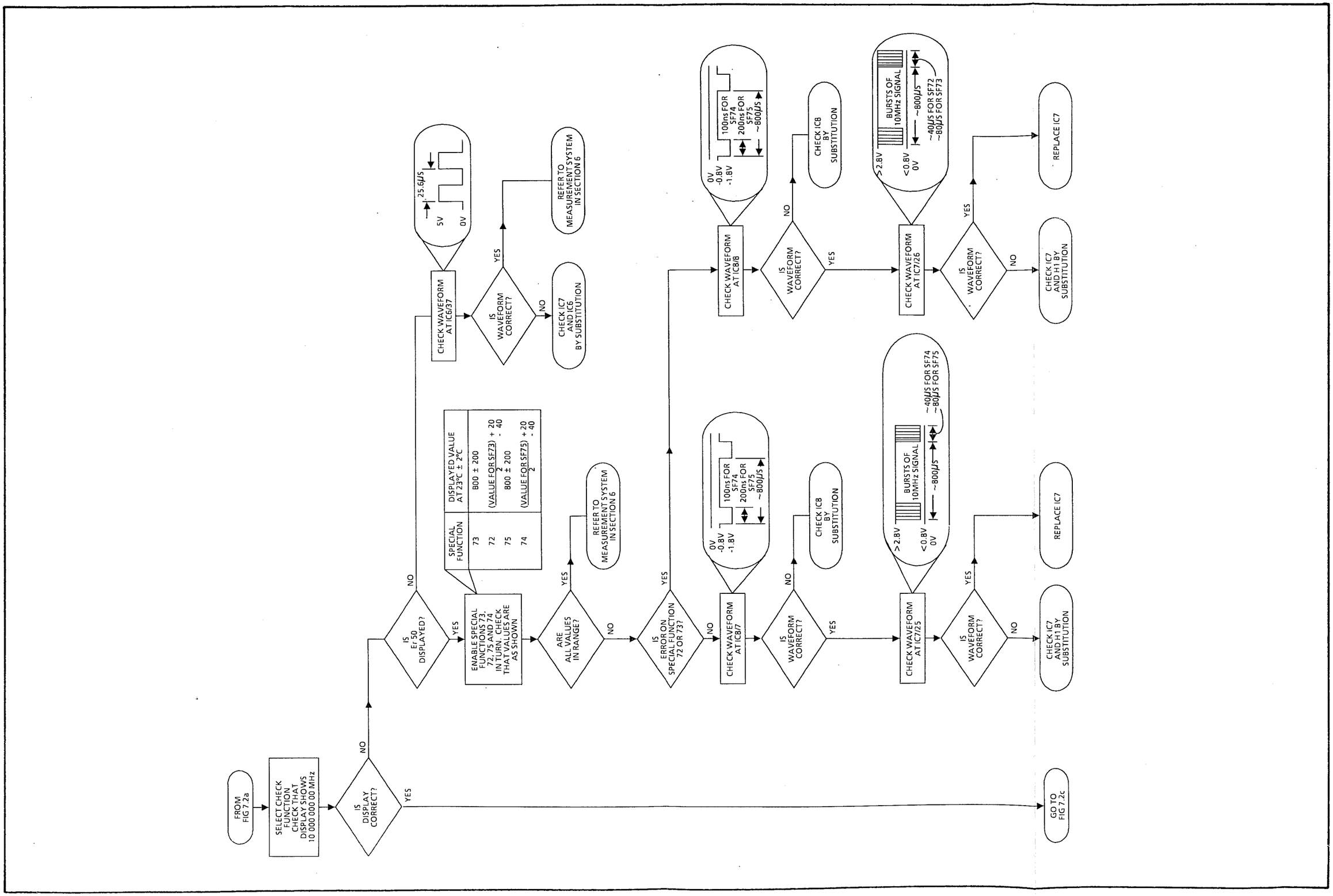


Fig. 7.2b Fault Finding Flowchart - Part 2

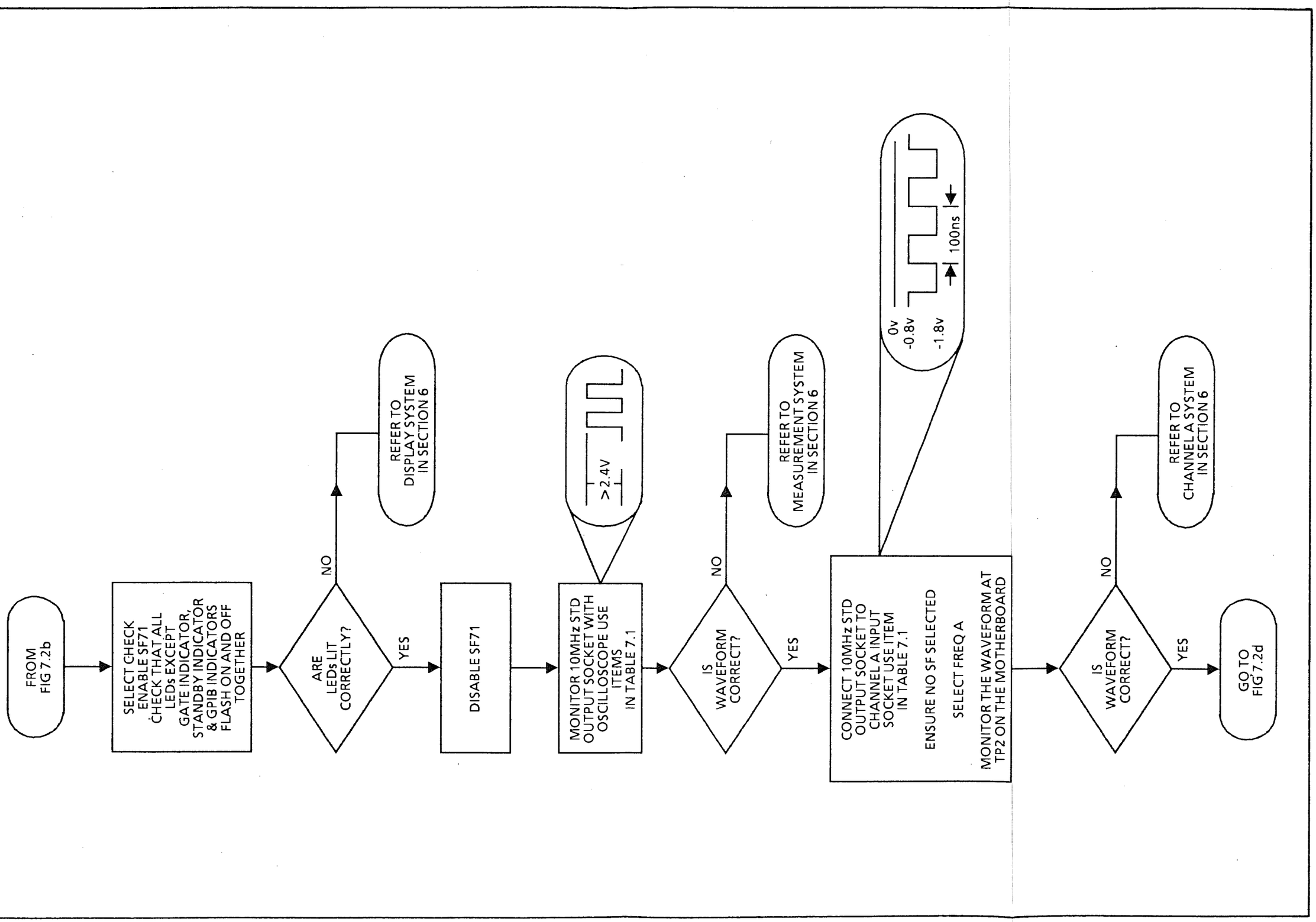


Fig. 7.2c Fault Finding Flowchart - Part 3

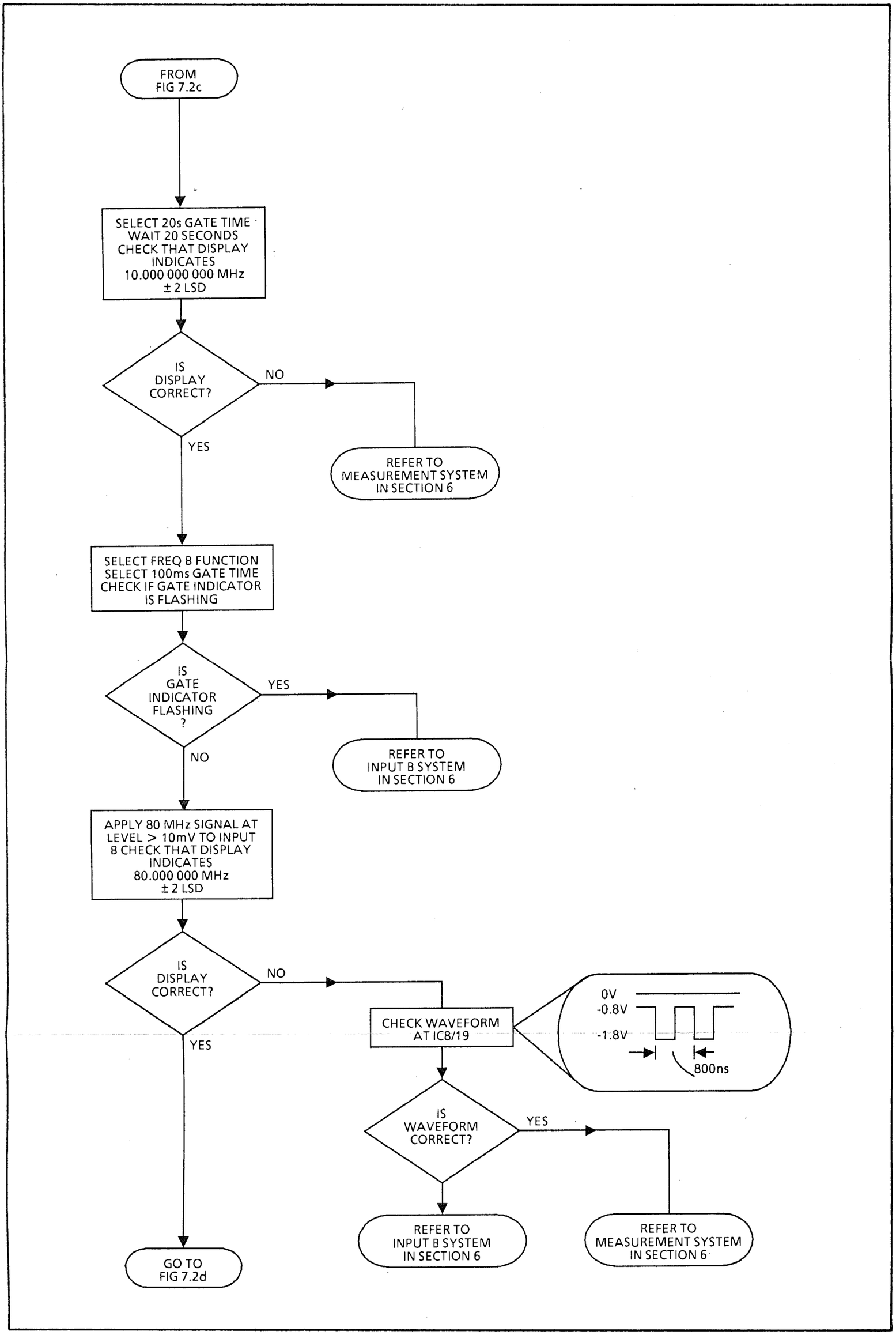


Fig. 7.2d Fault Finding Flowchart - Part 4

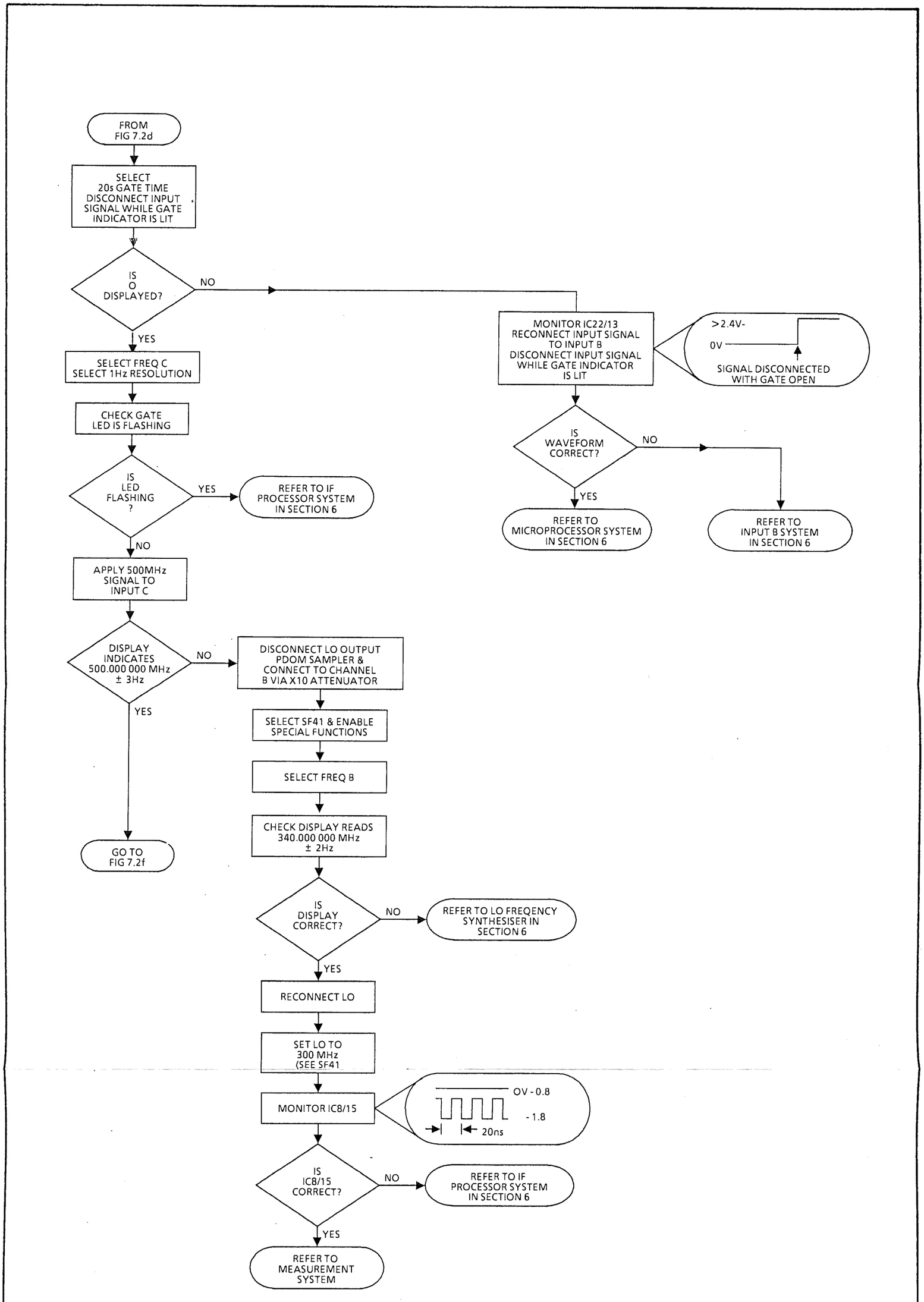


Fig. 7.2e Fault Finding Flowchart - Part 5

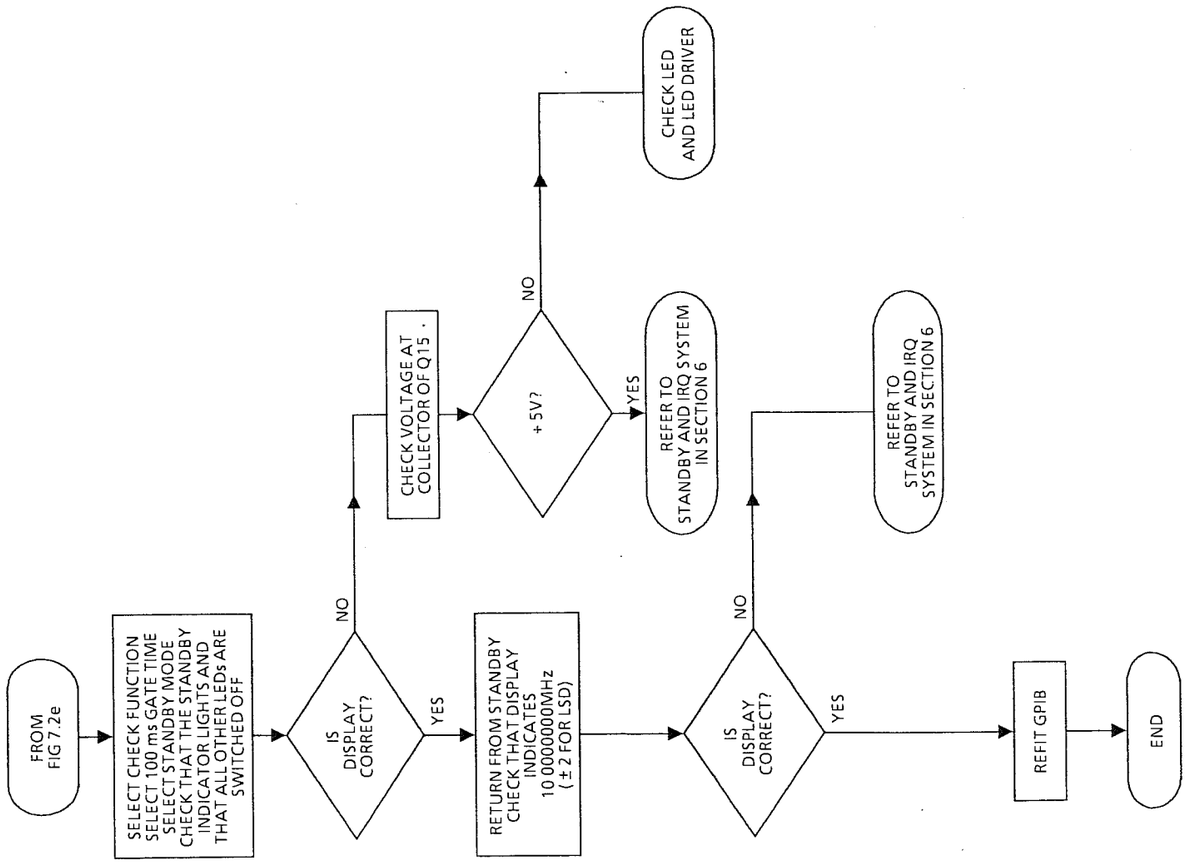


Fig. 7.2f Fault Finding Flowchart - Part 6

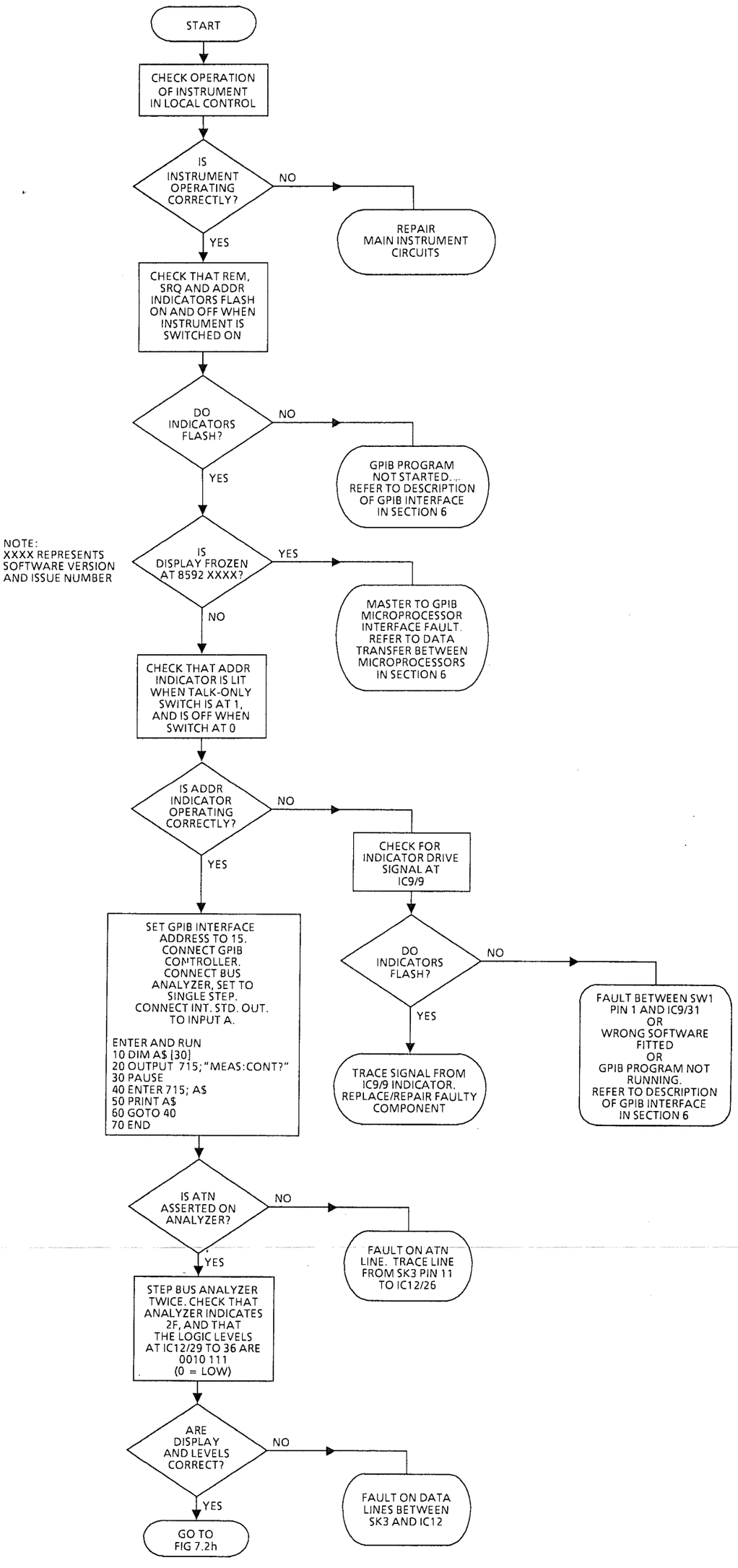


Fig. 7.2g Fault Finding Flowchart GPIB - Part 1

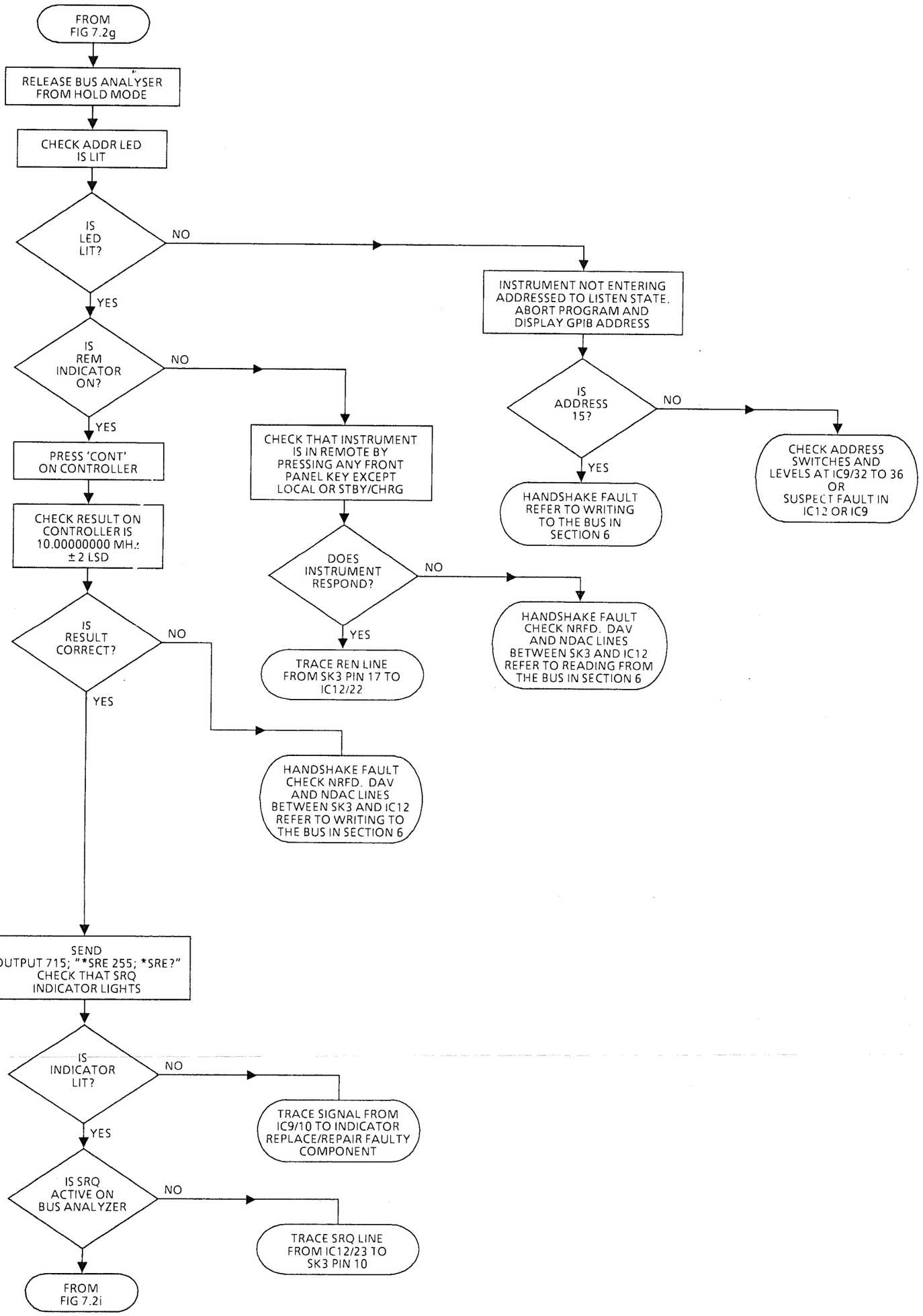


Fig. 7.2h Fault Finding Flowchart GPIB - Part 2

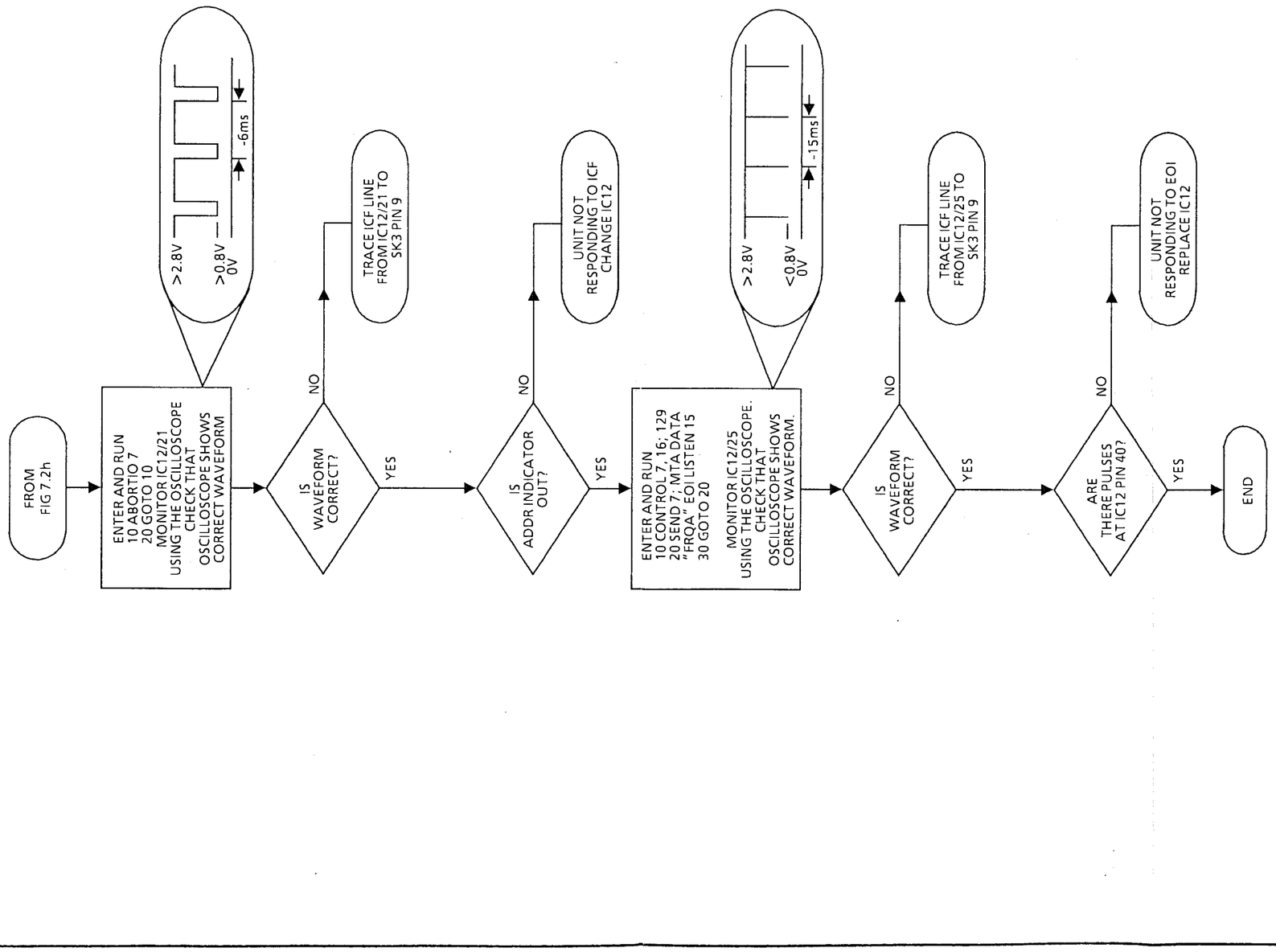


Fig. 7.2i Fault Finding Flowchart GPIB - Part 3

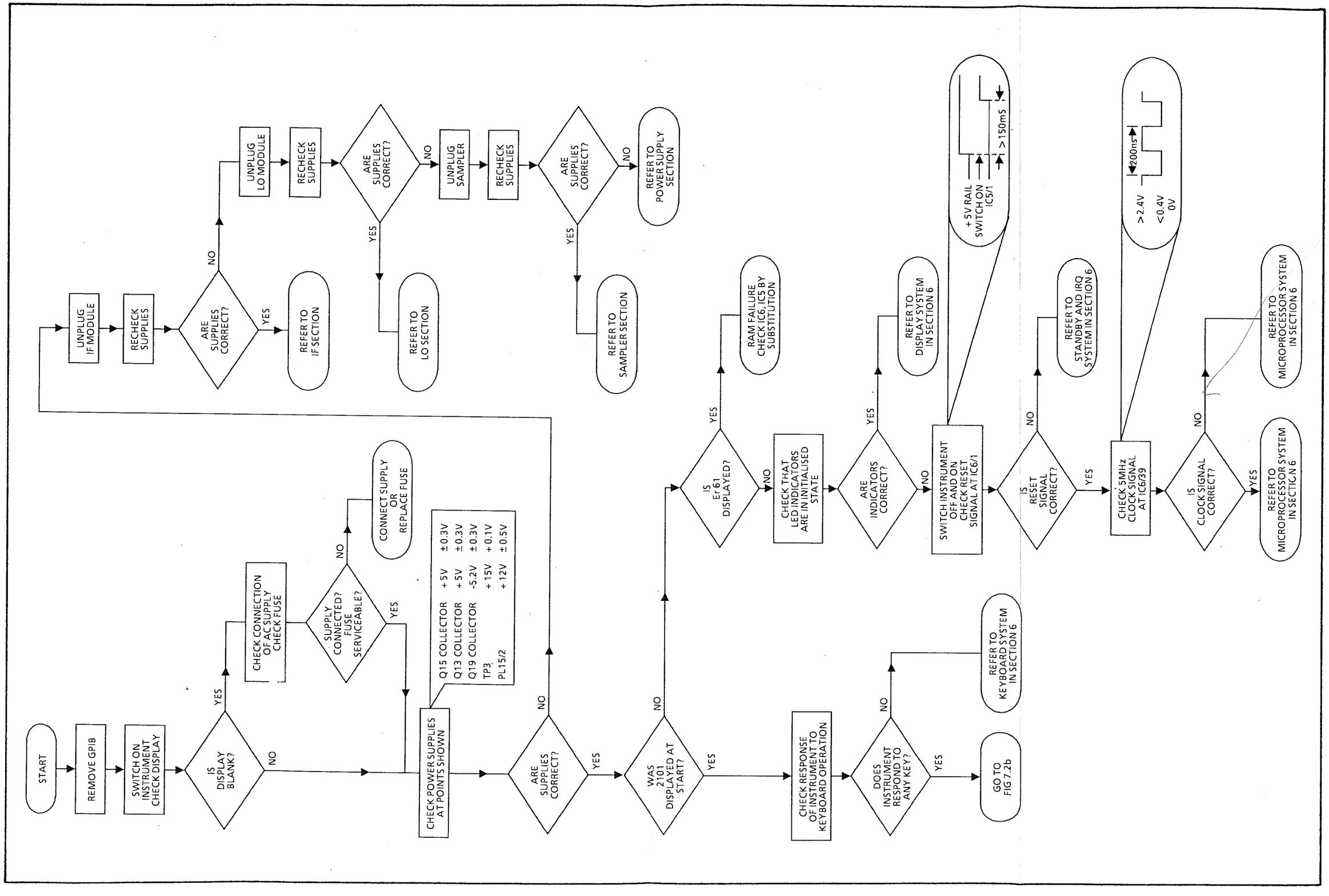


Fig. 7.2a Fault Finding Flowchart - Part 1

SETTING UP AFTER REPAIR

Introduction

39 After repair, the relevant setting-up procedures from those given in the following paragraphs should be implemented before carrying out the overall specification check. The procedures should also be used if the instrument fails a routine specification check.

40 The ambient temperature must be maintained at 23°C +/-2°C throughout the procedures. The instrument should be powered from an AC supply, not a battery pack.

WARNING: LETHAL VOLTAGES
THESE PROCEDURES REQUIRE THE INSTRUMENT TO BE OPERATED WITH THE COVERS REMOVED. LETHAL VOLTAGE LEVELS ARE EXPOSED UNDER THESE CONDITIONS.

+15 V Regulator (Located on Motherboard 19-3022)

41 Test equipment required:

Item	Table 7.1 Item No
Digital Multimeter	6
Probe	8
Adaptor	33

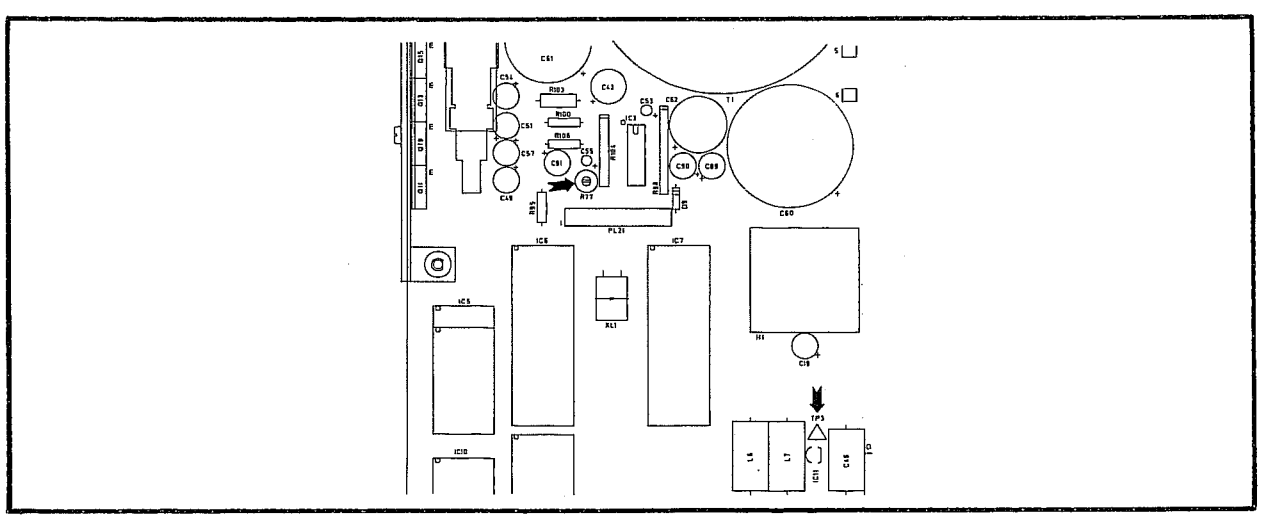


Fig. 7.3 Location of R77 and TP3

42 (1) Set R77 on the motherboard to mid position, see Fig. 7.3.

(2) Use the digital multimeter and probe to monitor the voltage between TP3 (+ve) and ground. Adjust R77 for +15 V +/-0.1 V.

(3) Disconnect the digital multimeter.

Input A System Sensitivity Adjustment

43 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	2
50 Ohms Through Termination	15
BNC(m)-BNC(m) Coax. Qty 2	18

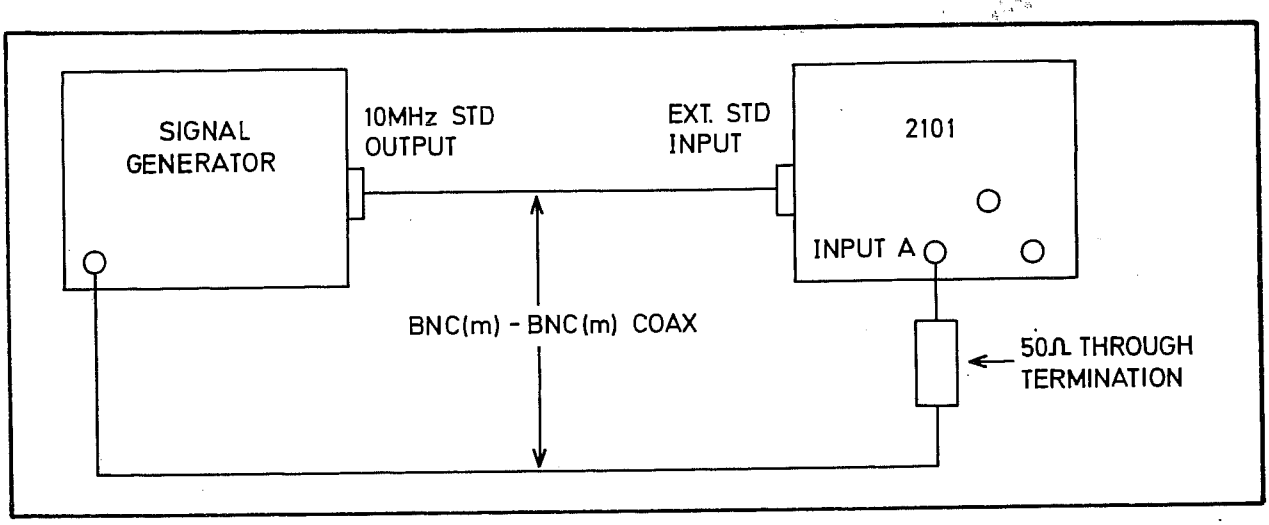


Fig. 7.4 Connections for Channel A Input System Adjustment

44 (1) Connect the test equipment as shown in Fig. 7.4.

(2) Set the signal generator to 80 MHz at 10 mV.

(3) On the 2101 select FREQ A. Verify that the EXT STD LED is lit, the GATE LED is flashing and the display reads 80 MHz. Set R7 on the motherboard fully counter-clockwise, see Fig. 7.5.

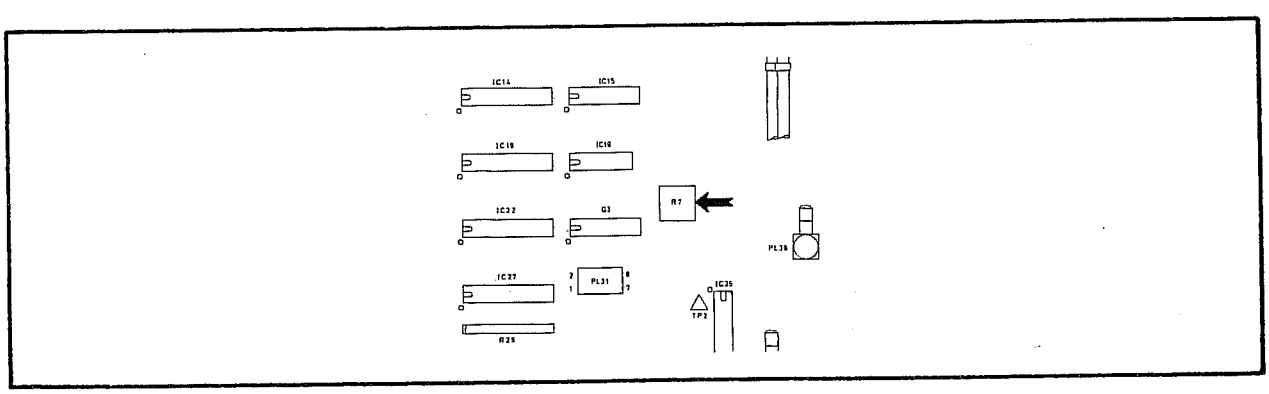


Fig. 7.5 Location of R7

(4) Adjust R7 slowly clockwise until the 2101 display becomes unstable. Turn R7 slowly counter-clockwise until the reading is just stable at 80 MHz +/-0.1 Hz.

(5) Reduce the output of the signal generator to 5 mV and verify that the GATE LED has stopped flashing. If not then repeat steps (4) and (5).

(6) Slowly increase the output from the signal generator until the reading on the 2101 is just stable at 80 MHz +/-0.1 Hz. Check that the generator output level is $\leq$13 mV. If not then repeat steps (2) to (6).

(7) Disconnect the test equipment.

Input B Prescaler Sensitivity Adjustment

45 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	2
BNC(m)-BNC(m) Coax. Qty 2	18

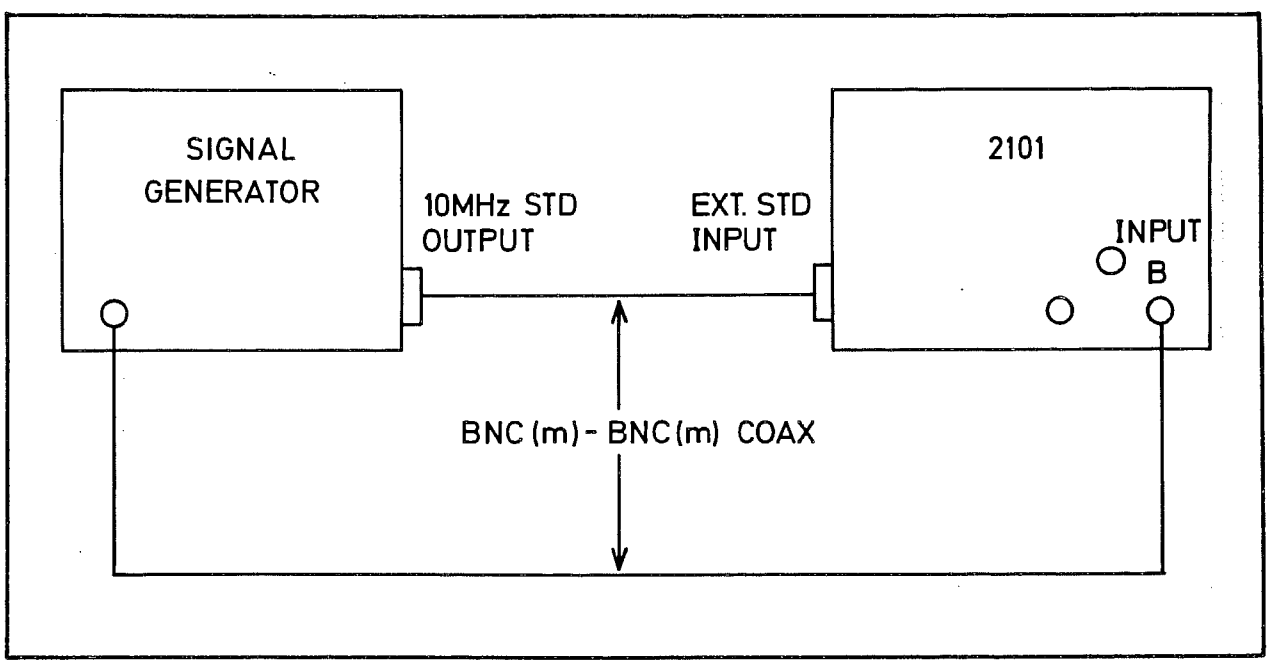


Fig. 7.6 Connections for Channel B Input System Adjustment

46 (1) Connect the equipment as shown in Fig. 7.6.

(2) Set the signal generator to 1 GHz at a level of 5 mV RMS.

(3) Set R27 on the prescaler assembly 19-3052 fully clockwise, see Fig. 7.7.

(4) On the 2101 select FREQ B and verify that the EXT STD LED is lit.

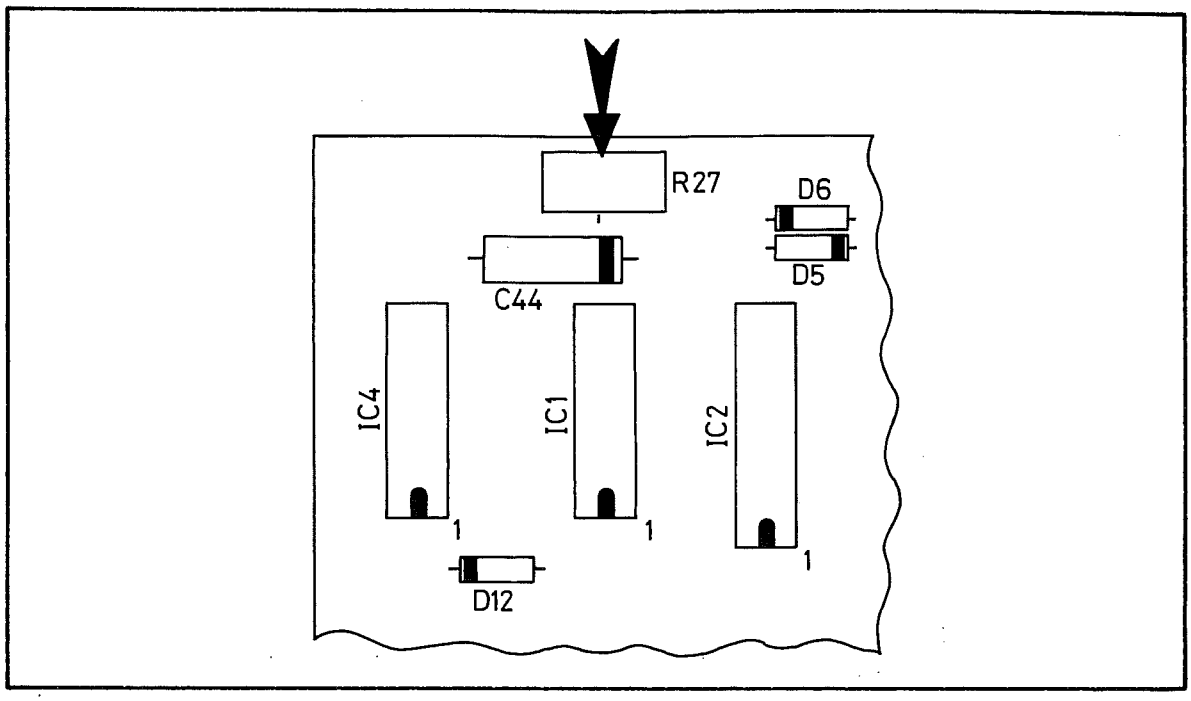


Fig. 7.7 Location of R27 on Prescaler Assembly

(5) Adjust R27 until the GATE LED just starts flashing. Check that the 2101 display reads 1000 MHz +/-1 Hz.

(6) Switch the generator output off. Set the signal generator output to 4.5 mV RMS. Switch the output of the generator on and verify that the 2101 is not counting, if it is then repeat steps (3) to (6).

(7) Disconnect the test equipment.

Channel C Input System

47 All the preset adjustments for the Input C system are contained within the LO Synthesizer module and the IF Processor module. These are dealt with separately in following sections.

48 The necessity for recalibration of a particular module is dictated by the nature of the repair. Two examples of this are as follows:

(1) A repair to the IF Processor module, or replacement of the Sampling Mixer module, does not require the recalibration of the LO Synthesizer module.

(2) A repair to the LO module may affect the LO drive level to the Sampling Mixer. This requires recalibration of the system gain preset, R14, housed within the IF Processor. The remaining IF Processor preset controls do not require recalibration.

The LO Module

49 Test equipment required:

Item	Table 7.1 Item No
Power Meter	5
Precision 20 dB Attenuator	14
BNC(f)-SMA(f) Adaptor	22
BNC(m)-SMC(m) Adaptor	23
Extended Ribbon Cable (LO)	28
Trimming Tool	32

50 (1) Switch the 2101 off. Remove the module stack to gain access to the LO Synthesizer module located underneath the IF Processor module. Use the extended ribbon cable to connect the module to the 2101. Position the stack to one side of the 2101.

(2) Disconnect the LO output coax at PL32/SK32 interface at the Sampling Mixer. Connect the equipment as shown in Fig. 7.8. Switch the 2101 on.

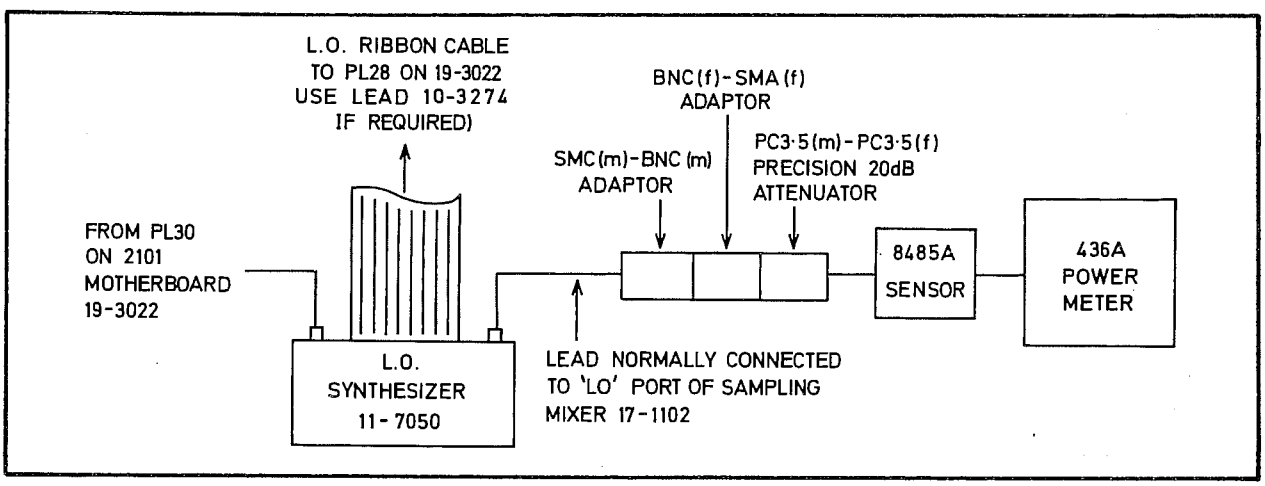


Fig. 7.8 Connections for Channel C Input System Adjustment (Pt. 1)

(3) On the 2101 select SF41 and SF37. This allows manual setting of the LO frequency and displays '0' if the LO Synthesizer is in lock, or '1' if it is out of lock.

(4) Now press:

3 2 5 SHIFT MHz STORE TRACK

This sets the LO frequency to 325 MHz. Check that the 2101 display reads '0'.

(5) Adjust R14 on the LO Synthesizer until the Power Meter reads +22 dBm +/-0.1 dBm. See Fig. 7.9 for the location of R14.

(6) Set the LO to each of the frequencies shown in Table 7.3 and check that the output level is as shown, and that the 2101 display reads '0'.

TABLE 7.3

LO Synthesizer Test Frequencies

Frequency (MHz)	Output Level (dBm)
292.5	+22 +/-1
300.0	+22 +/-1
310.0	+22 +/-1
320.0	+22 +/-1
330.0	+22 +/-1
340.0	+22 +/-1
350.0	+22 +/-1
354.5	+22 +/-1

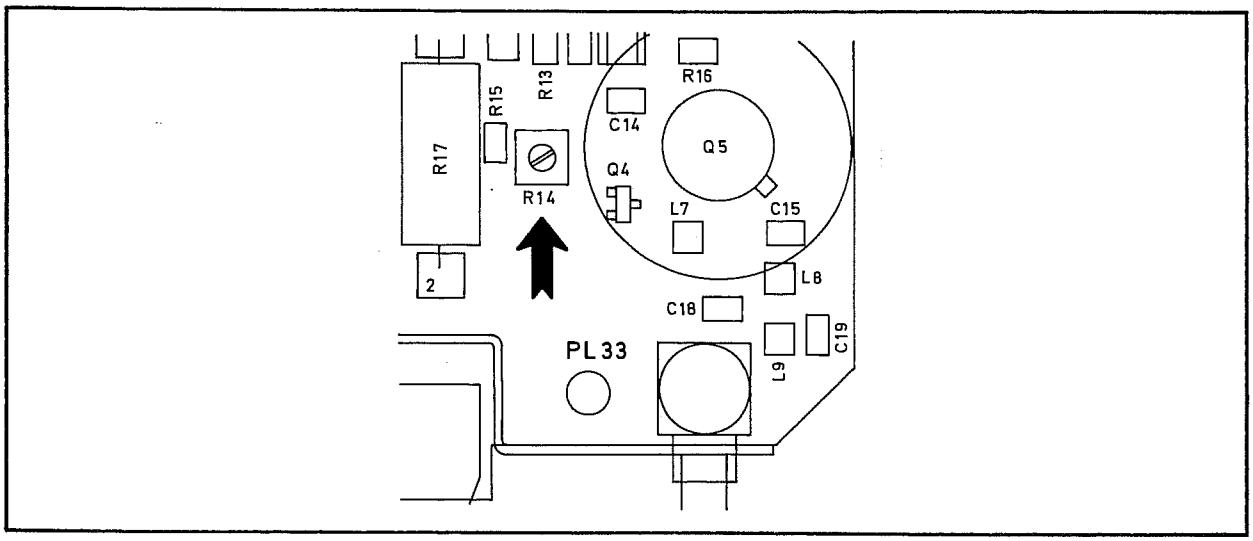


Fig. 7.9 Location of R14

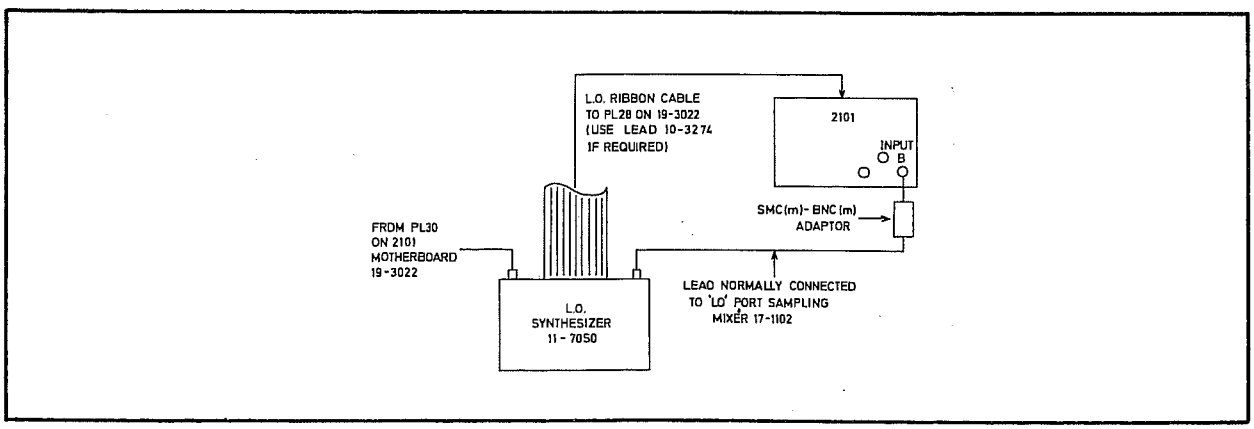


Fig. 7.10 Connections for Channel C Input System Adjustment (Pt. 2)

(7) Connect the equipment as shown in Fig. 7.10. On the 2101 select FREQ B. Set the LO to each of the frequencies shown in Table 7.3. At each step check that the frequency error is less than +/-2 Hz.

(8) Disconnect the test equipment.

The IF Processor Module

51 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	2
Power Meter	4
Digital Multimeter	6
x1 Probe for DMM	8
SMC(f)-SMC(f) Coax. x2	16
N(m)-SMC(m) Adaptor	19
N(f)-SMC(m) Adaptor	20
Extended Ribbon Cable (IF)	29
Trimming Tool	32
Adaptor	33
DC Block, Type 'N'	36 (Optional, see CAUTION)

52 (1) The module stack may be left fitted in the 2101 for these tests. Alternatively it can be removed from the 2101 and the IF Processor linked to the unit via the extended ribbon cable. Remove the lid of the IF Processor.

(2) Using the Digital Multimeter, check that the Sampling Mixer IF bias voltage at TP6 is +11 V +/-1 V relative to ground, see Fig. 7.11.

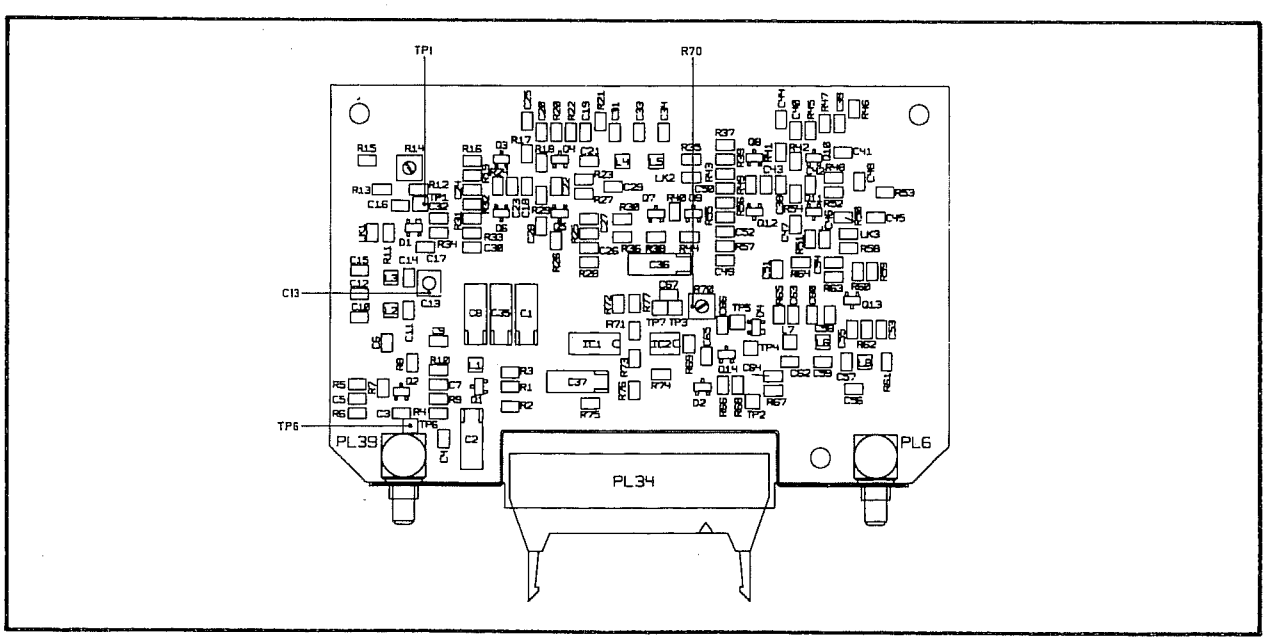


Fig. 7.11 Locations of TP1, TP6, R70 and C13

(3) Using the Digital Multimeter, check the IF level detector threshold voltage at TP1 is +150 mV +/-3 mV relative to ground. If necessary adjust R70 to achieve this voltage, see Fig. 7.11.

NOTE: If it is necessary to adjust R70, then the Input C sensitivity adjustment procedure should be followed, after the IF Processor calibration.

(4) Switch off the 2101. Disconnect the IF input and output coaxes at PL39 and PL6 on the IF module. Connect the equipment as shown in Fig. 7.12.

CAUTION: DC VOLTAGES ON THE IF PROCESSOR MODULE THE SIGNAL GENERATOR MAY BE DAMAGED BY DC VOLTAGES AT ITS OUTPUT. IF THIS IS SO THEN CONNECT THE AC COUPLER (TEST EQUIPMENT LIST ITEM 36) BETWEEN THE SIGNAL GENERATOR AND THE IF PROCESSOR.

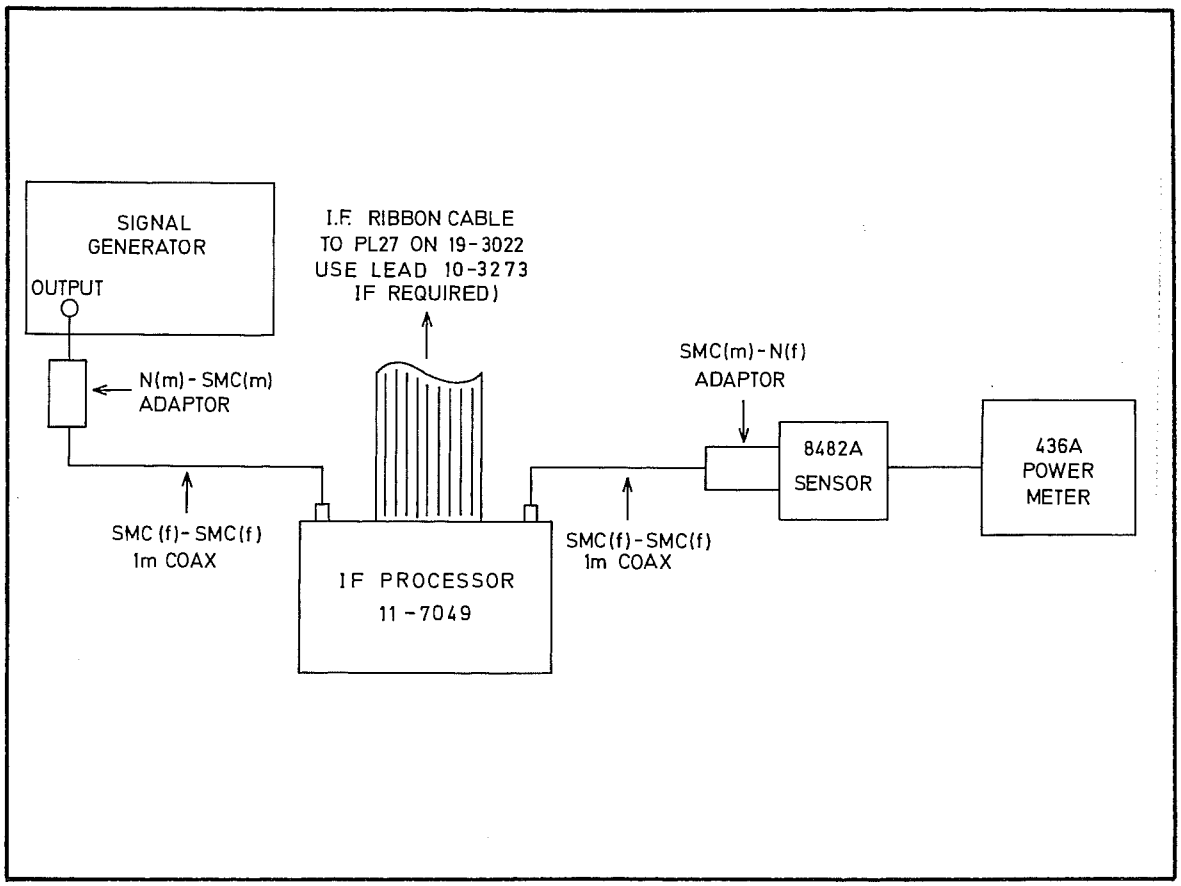


Fig. 7.12 Connections for Channel C Input System Adjustment (Pt. 3)

(5) Set the signal generator to 184 MHz at -6 dBm.

(6) On the 2101 select SF41 and SF36. This configures the 2101 to monitor and display the status of the IF BW line from the IF Processor module. It is a calibration aid to assist in setting up the 175 MHz low pass filter.

(7) Adjust C13 slowly until the 2101 display just changes from '0' to '1', see Fig. 7.11. This sets the stopband edge of the 175 MHz low pass filter.

(8) Set the generator to the frequencies shown in Table 7.4, and check the 2101 display status. This checks the adjustments of the stopband edge of the 175 MHz low pass filter. If the results are incorrect then repeat the procedure in step (7) until the status is correct.

TABLE 7.4

175 MHz Low Pass Filter Test Frequencies

Frequency (MHz)	2101 Display Status
183.5	1
184.5	0

(9) On the 2101 select SF35. This causes the 2101 to display the status of the IF level detector.

(10) Set the signal generator to 80 MHz and adjust its output level until the 2101 display just changes from '0' to '1'. Check that the output from the signal generator is -55 dBm +/-5 dB. Note this level as 'P.in'. Check that the power meter reads -5 dBm +/-2 dB and note the actual level as 'REF'.

(11) To check the flatness of response of the IF Processor to the IF COUNT output, proceed as follows. Set the signal generator to the frequencies shown in Table 7.5 and at each frequency maintain the output level at 'P.in'. Check for the appropriate IF output level at PL6, in dBm relative to the REF output level at 80 MHz.

TABLE 7.5

IF Processor Output Response

Frequency (MHz)	IF Output Level (dBm)
0.5	REF +/-2
41.0	REF +/-2
112.0	REF +/-2
174.0	REF +/-2
194.0	Less than (REF -6)

(12) To check the passband flatness of the IF level detector proceed as follows. Set the signal generator to each of the frequencies shown in Table 7.6. At each frequency apply the output level step shown and check for the corresponding display on the 2101.

TABLE 7.6

IF Level Detector Passband Response

Frequency (MHz)	Step From	Step To	2101 Display
41	Off	(P.in -2 dB)	0
41	(P.in -2 dB)	(P.in +2 dB)	1
112	Off	(P.in -2 dB)	0
112	(P.in -2 dB)	(P.in +2 dB)	1

(13) To check the IF level detector bandwidth proceed as follows. Set the signal generator to each of the frequencies shown in Table 7.7. At each frequency apply the level or level step shown and check for the corresponding display on the 2101.

TABLE 7.7

IF Level Detector Bandwidth

Frequency (MHz)	Level or Level Step	2101 Display
26	From Off to (P.in +3 dB)	0
30	(P.in +3 dB)	1
133	From Off to (P.in +3 dB)	0 *
123	(P.in +3 dB)	1 **

* If '1' is displayed at 133 MHz, replace C62 on assembly 19-3024 with 27 pF and repeat Test (13).

** If '0' is displayed at 123 MHz, replace C62 on assembly 19-3024 with 18 pF and repeat Test (13).

(14) To check the IF Mute function proceed as follows. On the 2101 select SF43, this mutes the IF COUNT output. Set the signal generator to 80 MHz at -7 dBm and check that the power meter reads 'UNDERRANGE'.

Input C Sensitivity

53 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1
Power Meter	5
Precision Power Splitter	13
20 dB Attenuator	14
PC3.5(m)-PC3.5(m) Coax.	17
BNC(m)-BNC(m) Coax.	18
N(m)-SMA(m) Adaptor	21 *
PC3.5(m)-PC3.5(m) Adaptor	35 **

NOTE: * Not required if Rear Inputs Option 01 is fitted.
** Only required if Rear Inputs Option 01 is fitted.

Without Power Limiter Option 11

54 (1) Connect the equipment as shown in Fig. 7.13, (Fig. 7.14 if Rear Inputs Option 01 is fitted).

(2) On the 2101 select SF35 and SF41. Set the LO to 340 MHz by pressing:

3 4 0 SHIFT MHz STORE TRACK

and set N to -37 by pressing:

3 7 SHIFT +/- SHIFT STORE LOW FM

NOTE: At switch-on the 2101 already has these set as default values.

(3) Set the signal generator to 12.5 GHz and adjust its output level for a reading of -15 dBm, on the power meter.

(4) Adjust R14 on the IF Processor module clockwise until the 2101 display just changes from '0' to '1'.

(5) Reduce the output from the generator for a reading of -16 dBm on the power meter. Check that the 2101 display shows '0'.

(6) Slowly increase the signal generator output level until the 2101 display just changes from '0' to '1'. Check that the power meter reads -15 dBm +/-0.2 dB.

(7) Disconnect the test equipment.

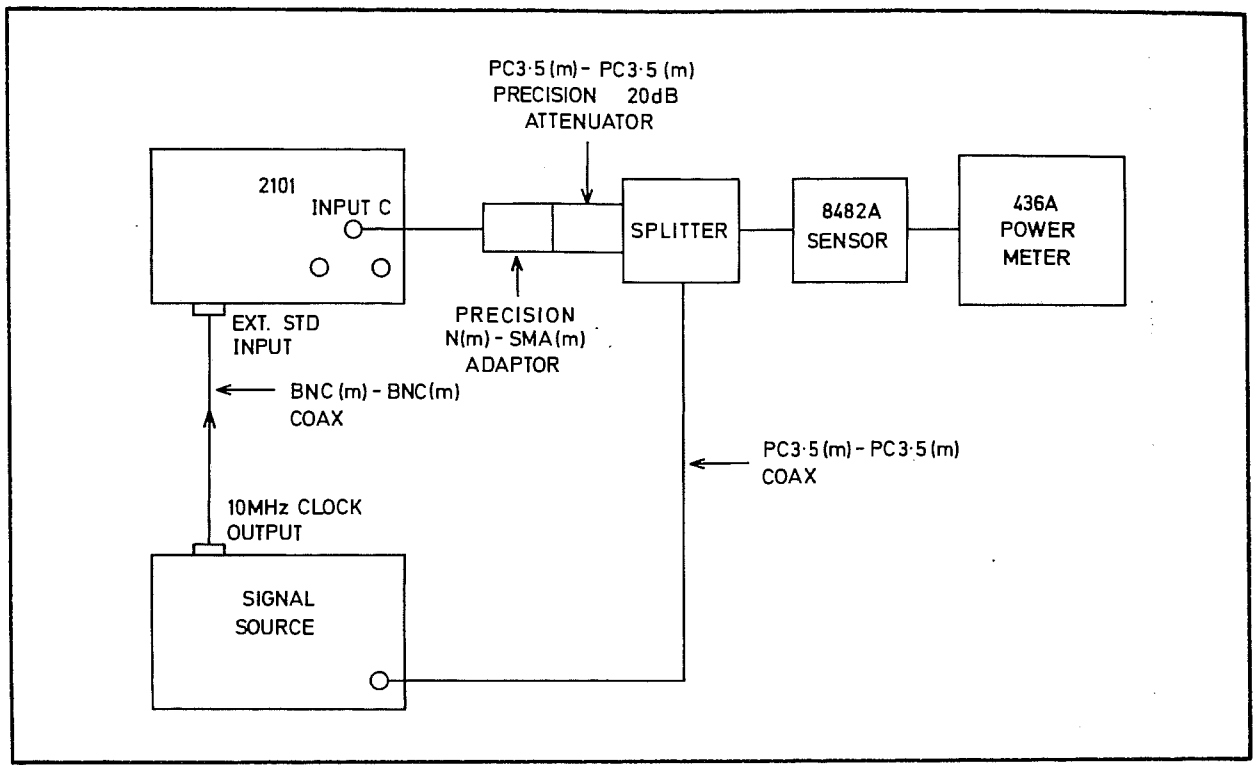


Fig. 7.13 Connections for Channel C Input System Adjustment (Without Rear Inputs Option 01)

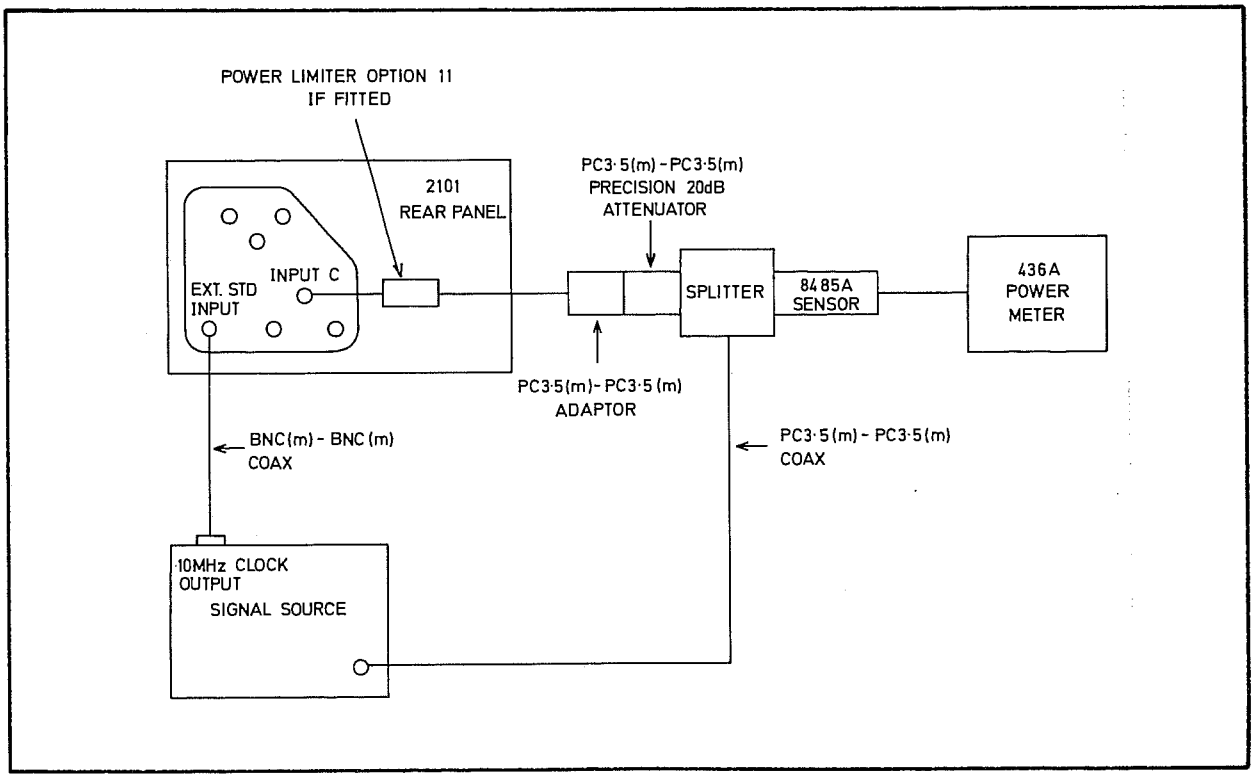


Fig. 7.14 Connections for Channel C Input System Adjustment (With Rear Inputs Option 01 Fitted)

With Power Limiter Option 11 Fitted

55 (1) Connect the equipment as shown in Fig. 7.13, (Fig. 7.14 if Rear Inputs Option 01 is fitted).

(2) On the 2101 select SF35 and SF41. Set the LO to 340 MHz by pressing:

3 4 0 SHIFT MHz STORE TRACK

and set N to -37 by pressing:

3 7 SHIFT +/- SHIFT STORE LOW FM

NOTE: At switch-on the 2101 already has these set as default values.

(3) Set the signal generator to 12.5 GHz and adjust its output level for a reading of (-15 + CAL)dBm, on the power meter, where 'CAL' is the calibration (insertion loss) factor printed on the limiter module.

(4) Adjust R14 on the IF Processor module clockwise until the 2101 display just changes from '0' to '1'.

(5) Reduce the output from the generator for a reading of (-16 + CAL)dBm, on the power meter. Check that the 2101 display shows '0'.

(6) Slowly increase the signal generator output level until 2101 display just changes from '0' to '1'. Check that the power meter reads (-15 + CAL)dBm +/-0.2 dBm.

(7) Disconnect the test equipment.

Frequency Doubler 19-1238 (Options 04A and 04B only)

56 Test equipment required:

Item	Table 7.1 Item No
Oscilloscope	7
Probe	8
Trimming Tool	32

57 (1) Switch on the 2101. Allow a warm-up period of 10 minutes for option 04A and 30 minutes for option 04B.

(2) Monitor the signal at pin 3 using the oscilloscope and x10 probe. Verify that the frequency is 10 MHz.

(3) If necessary, adjust T1 and T2 to obtain a signal level not less than 0.5 V peak-to-peak.

(4) Monitor the DC voltage at TP1 using the oscilloscope and x10 probe. Adjust T1 and T2 to obtain the smallest possible voltage. Verify that the voltage achieved is in the range from 400 mV to 800 mV.

(5) Transfer the probe to pin 3. Verify that the signal frequency is 10 MHz and that the level is in the range from 0.8 V to 1.2 V.

(6) Disconnect the test equipment.

Reference Frequency Multiplier Option 19-1164 (Option 10)

58 Test equipment required:

Item	Table 7.1 Item No
Oscilloscope	7
Probe	8
Frequency Standard	9
BNC(m)-BNC(m) Coax.	18
Trimming Tool	32

59 (1) Switch the 2101 on.

(2) Connect the frequency standard to the EXT. STD. INPUT socket. Verify that the EXT STD indicator lights.

(3) Monitor the DC voltage at TP1 using the oscilloscope and x10 probe.

(4) If necessary, adjust C2 to obtain a voltage of +2.5 V +/-0.2 V.

(5) Switch off the 2101. Disconnect the test equipment.

Battery Pack 11-9009 (OPTION 07)

60 Test equipment required:

Item	Table 7.1 Item No
Digital Multimeter (Qty. 2)	6
DC Power Supply	12
Ext. DC Input Lead	27

NOTE:

(1) The battery pack should be installed in the parent 2101.

(2) The battery tray should be in position, but the flying lead (SK12/PL12) should be disconnected.

(3) Take care to connect the test equipment to the points specified. Connection must be made to PL21 from the underside of the motherboard.

61 Connect the test equipment as shown in Fig. 7.15. DO NOT CONNECT THE 2101 TO AN AC SUPPLY.

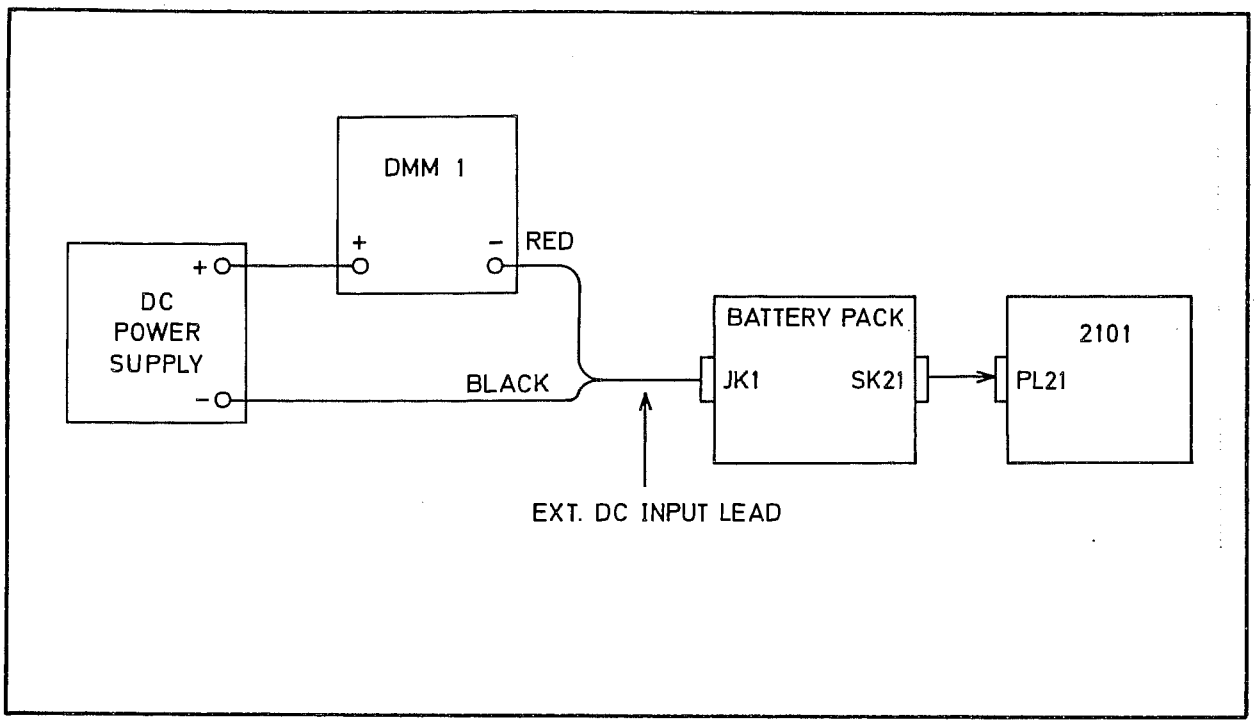


Fig. 7.15 Connections for Battery Pack Test

62 (1) Set R10, R28 and R36 on the battery pack fully clockwise, see Fig. 7.16.

(2) Set the INTERNAL/EXTERNAL switch to EXTERNAL.

(3) Set the NORMAL/BATTERY SAVE switch to NORMAL.

63 (1) Set DMM 1 to measure direct current greater than 2 A.

(2) Set the power supply output to 15 V.

(3) Switch on the 2101. Verify that the normal start-up sequence occurs.

64 (1) Set DMM 2 to measure over the range from 4 V to 20 V DC.

(2) Connect DMM 2 between PL21 pin 5 (Positive) and PL21 pin 10 (0 V).

(3) If necessary, adjust R28 on the battery pack to obtain an indication of between 5.54 V and 5.56 V.

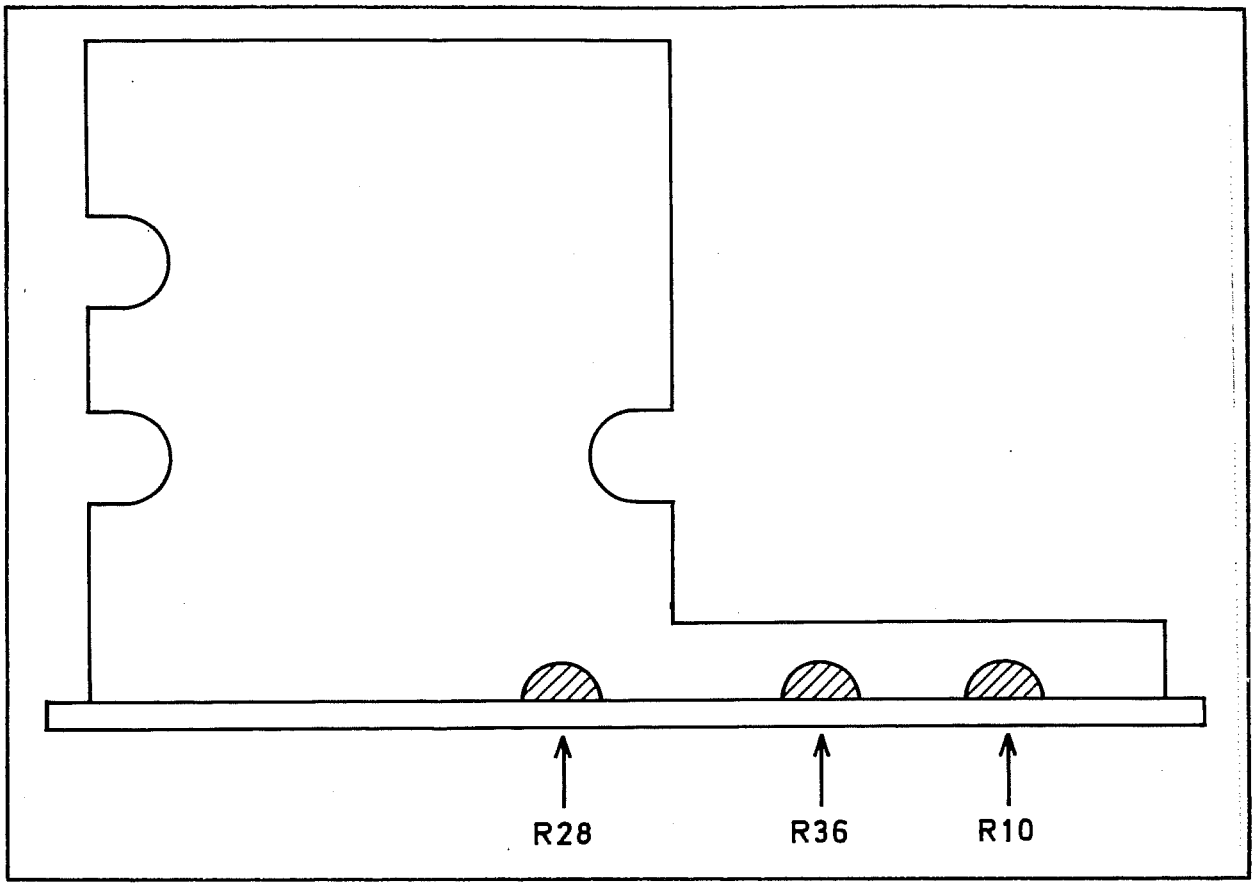


Fig. 7.16 Locations of R10, R28 and R36

65 Use the DMM to measure the voltage between PL21 pin 10 (0 V) and each of the points shown in Table 7.8. Verify that the voltages measured are as shown in column A.

TABLE 7.8

Battery Pack Voltage Levels

Test Point	Voltage Relative to PL21 Pin 10	
	A	B
PL21 pin 5	+5.54 V to +5.56 V	+5.52 V to +5.56 V
PL21 pin 6	-5.7 V to -6.1 V	-5.65 V to -6.15 V
PL21 pin 18	+16.8 V to +17.6 V	+16.7 V to +17.7 V

66 Transfer the digital multimeter to measure the voltage between PL21 pin 21 (positive) and PL21 pin 10 (0 V). Adjust the power supply output to obtain an indication of 10.0 V to 10.2 V.

67 Use DMM 2 to measure the voltage between PL21 pin 10 (0 V) and each of the points in Table 7.8. Verify that the voltages measured are as shown in column B.

68 (1) Turn R10 slowly counter-clockwise until the 2101 shuts down completely (all display LEDs go out).

(2) Verify that the current drawn from the power supply immediately after the 2101 shuts down, as indicated on DMM 1, is less than 10 uA (reduce the DMM range as required).

(3) Reset DMM 1 to measure direct current greater than 2 A.

69 (1) Connect DMM 2 between PL12 pin 1 (positive) and PL12 pin 3 (negative).

(2) Restore the power supply output to 15 V.

(3) Switch the 2101 off and on. Wait until the start-up sequence is completed.

(4) Verify that DMM 2 indicates not more than 0.1 V

(5) Switch the 2101 to standby.

(6) Adjust R36 on the battery pack until the digital multimeter indicates between 7.62 V and 7.64 V.

(7) Switch the 2101 off. Disconnect DMM 2.

70 (1) Set DMM 2 to measure direct current greater than 1.5 A.

(2) Connect DMM 2 between PL12 pin 1 (positive) and PL12 pin 3 (negative).

(3) Disconnect the DC power supply and DMM 1. Connect the 2101 to a suitable AC supply.

(4) Switch the 2101 on. Wait until the start-up sequence is completed.

(5) Switch the 2101 to standby. Verify that the current between PL12 pin 1 and PL12 pin 3 is between 0.9 A and 1.1 A.

(6) Switch the 2101 off.

71 (1) Disconnect DMM 2 from PL12.

(2) Connect the battery at PL12/SK12.

(3) Select INTERNAL. If necessary, switch the 2101 on and select standby to charge the battery. Switch the 2101 off.

(4) Disconnect the 2101 from the AC supply.

(5) Switch the 2101 on. Verify that the instrument can be switched in and out of STANDBY.

(6) Switch the 2101 off. Lock R10, R28 and R36 with a small quantity of silicone rubber.

INTERNAL FREQUENCY STANDARD, ROUTINE CALIBRATION

72 Test equipment required:

Item	Table 7.1 Item No
Frequency Standard	9
BNC(m)-BNC(m) Coax.	18

NOTE: If an Option 04A (9444) or Option 04B (9423) frequency standard is fitted, allow the instrument to warm up for 24 hours (switched to STANDBY, if required) before making any adjustment.

73 (1) Switch on the 2101. Select FREQ A and verify that '000 000 000' is displayed.

(2) Connect the test equipment as shown in Fig. 7.17.

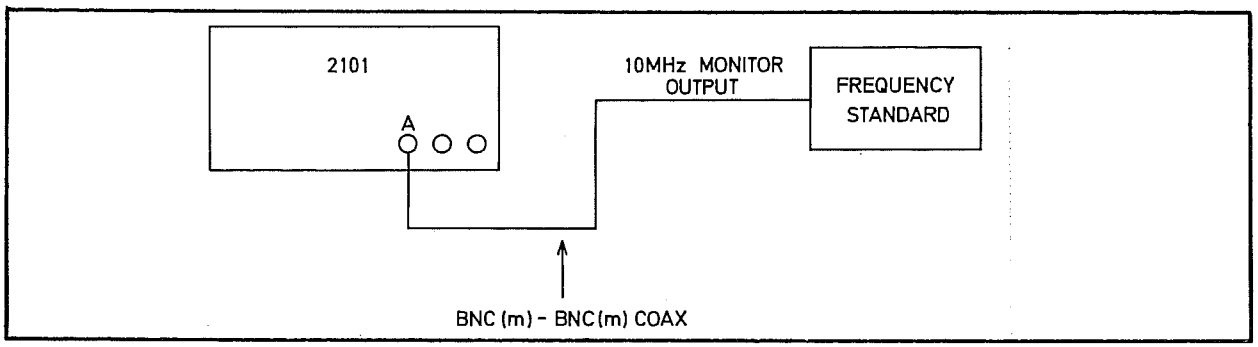


Fig. 7.17 Connections for Internal Frequency Standard Adjustment

(3) Press 1 0 SHIFT MHz STORE OFFSET

(4) Press SHIFT RECALL OFFSET

Verify that 10.0000000000 MHz is displayed.

(5) Press CONTINUE and SHIFT OFFSET

This causes the display to show frequency difference.

(6) Adjust the internal frequency standard, via the aperture in the rear panel, to be as near to 10 MHz as possible (i.e. the display as close to 0 as possible). The display limits are shown in Table 7.9.

(7) Switch off the 2101. Switch off and disconnect the test equipment.

TABLE 7.9

Internal Frequency Standard Accuracy

Frequency Standard	Display	Equivalent Accuracy
Standard Oscillator	+/-5 Hz	5 parts in 10^7
Option 04T	+/-1 Hz	1 part in 10^7
Option 04A (9444)	+/-0.1 Hz	1 part in 10^8
Option 04B (9423)	+/-0.01 Hz	1 part in 10^9

OVERALL SPECIFICATION CHECK

Introduction

74 Satisfactory completion of the following performance verification procedures (PVPs) will confirm that the instrument is functional and meets its specification. Before commencing the specification check ensure that the instrument passes the test given in Section 3 paragraphs 9 and 10. The PVPs should be carried out in the order given.

75 The following conditions must be maintained throughout the specification check:

(1) The instrument must be operated from an AC supply.

(2) The line voltage must be within the range indicated by the line voltage selector.

(3) The instrument covers must be fitted.

(4) The ambient temperature must be 23°C +/-2°C.

(5) The power supply to the frequency standard must be uninterrupted.

76 The instrument should be allowed to warm up for one hour (switched to standby if required) before commencing the specification check. If Option 04A or 04B is fitted, allow the instrument to warm up for 24 hours.

Input A Sensitivity PVP

77 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	2
Synthesized Audio Source	3 *
OR	
Non-synthesized Audio Source	34 *
50 Ohms through termination	15
BNC(m)-BNC(m) Coax. Qty 2	18 **

* Choice governed by extent of AF testing required. See AF Sensitivity PVP.

** Only one required when using non-synthesized audio source.

RF Sensitivity PVP

78 (1) Connect the equipment as shown in Fig. 7.18. Check that the EXT STD indicator is lit.

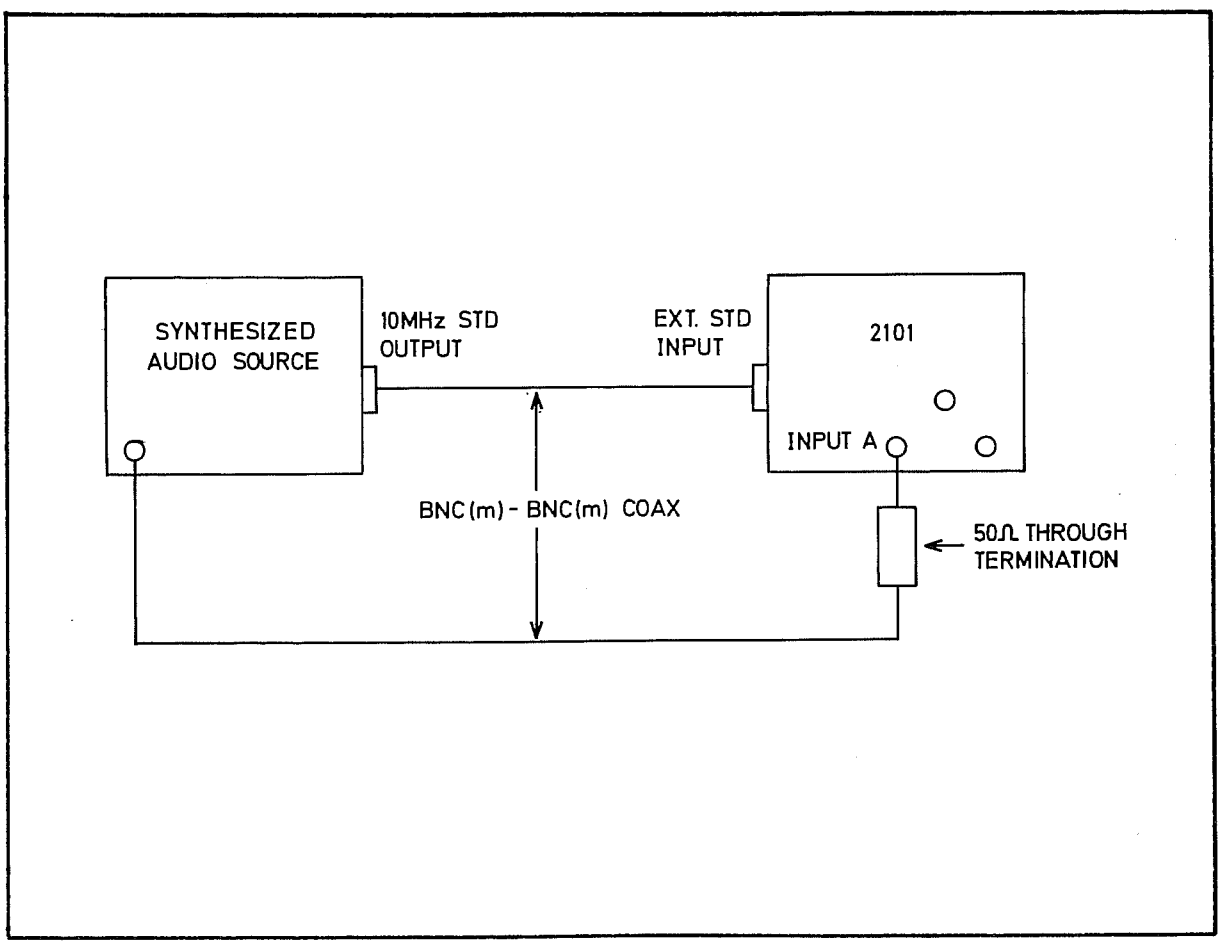


Fig. 7.18 Connection for RF Sensitivity PVP

(2) To set a 0.5 second gap between measurements on the 2101, press:

. 5 SHIFT STORE SAMPLE

(3) Set the signal generator to the frequencies shown in Table 7.10, and on the 2101 set the appropriate resolution.

TABLE 7.10

RF Sensitivity PVP Accuracy

Frequency (MHz)	Set Resolution	Allowable Error	Sensitivity (mV RMS)
80 MHz	8 digits	+/-2 Hz	18
10 MHz	7 digits	+/-2 Hz	18
100 kHz	5 digits	+/-3 Hz	18

(4) At each step measure the actual sensitivity of the 2101 and check that this is not worse than the figure shown.

(5) Disconnect the test equipment.

AF Sensitivity PVP

79 Two methods are described. The first uses a synthesized audio source and gives a true check of the 2101 count accuracy. The second uses a non-synthesized audio source and appraises the 2101 count jitter but not absolute accuracy.

AF Sensitivity PVP (Method 1, using synthesized audio source)

80 Use of the synthesized audio source allows the absolute count accuracy of the 2101 Input A to be checked.

(1) Connect the equipment as shown in Fig. 7.19. Check that the EXT STD indicator is lit.

(2) On the 2101 select SF11 to enable the 50 kHz filter and set a 0.5 second gap between measurements by pressing:

. 5 SHIFT STORE SAMPLE

(3) Set the AF Source to the frequencies shown in Table 7.11 and set the appropriate resolution on the 2101.

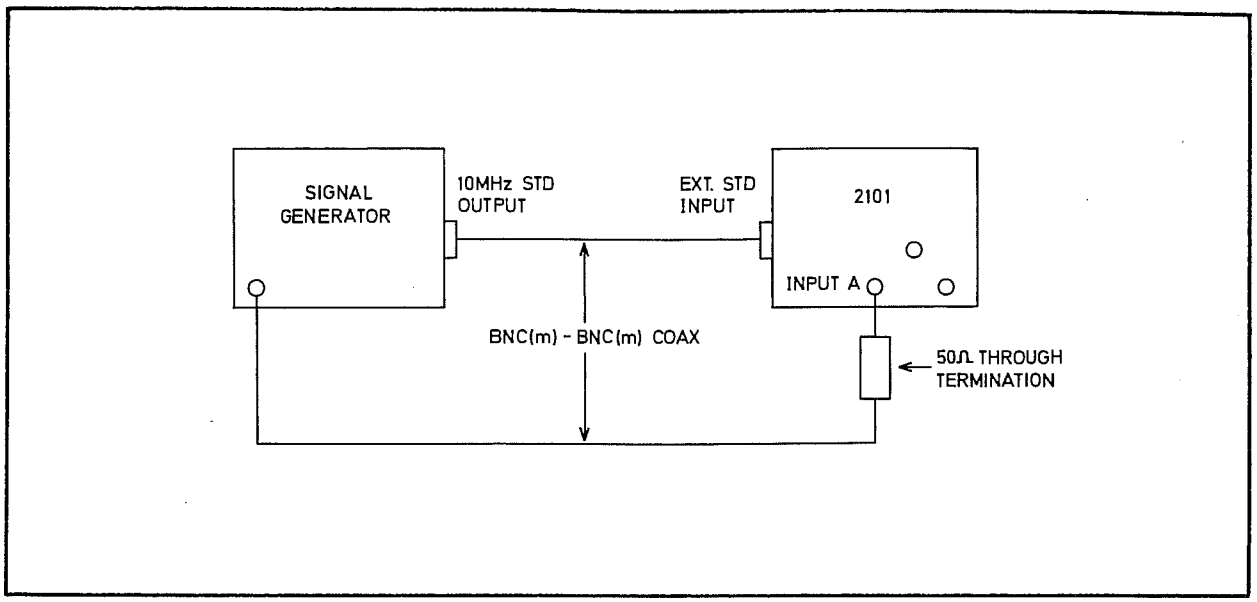


Fig. 7.19 Connection for AF Sensitivity PVP (Method 1)

TABLE 7.11

AF Sensitivity PVP Accuracy

Frequency	Set Resolution	Allowable Error	Sensitivity (mV RMS)
5 kHz	6 digits	+/-1.3 Hz	18
10 kHz	3 digits	+/-1.3 Hz	18

(4) At each step measure the actual sensitivity of the 2101 and check that this is not worse than the figure shown.

(5) Disconnect the test equipment.

AF Sensitivity PVP (Method 2, using non-synthesized audio source)

81 Use of the non-synthesized audio source will not allow the absolute count accuracy of the 2101 Input A to be checked. It will, however, allow 2101 measurement jitter to be appraised. Due allowance should be made for drift and jitter of the particular source used.

(1) Connect the equipment as shown in Fig. 7.20. Check that the EXT STD indicator is lit.

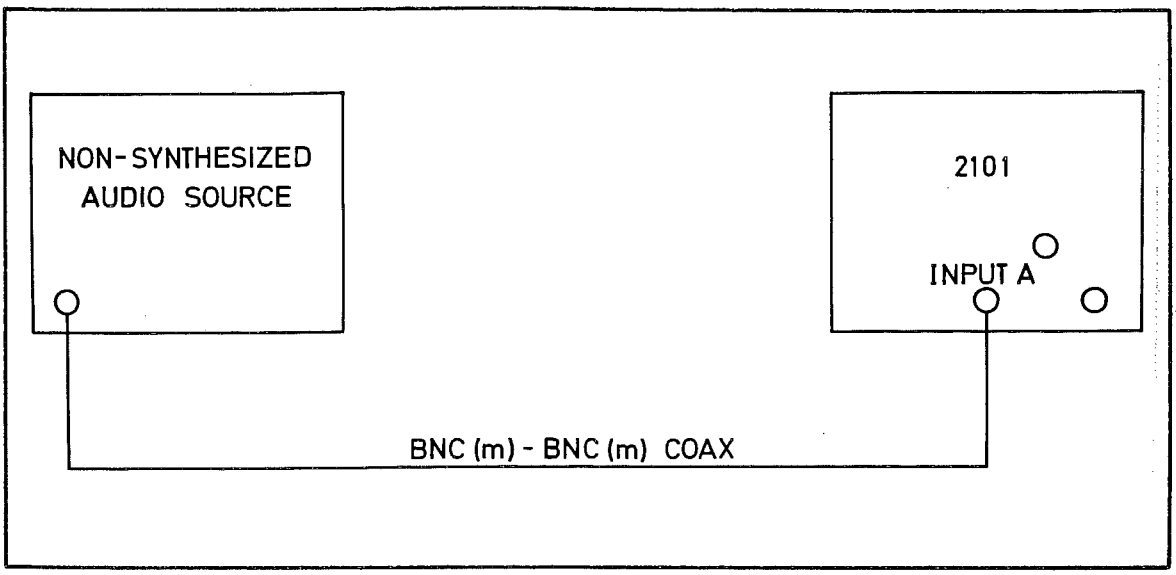


Fig. 7.20 Connection for AF Sensitivity PVP (Method 2)

(2) On the 2101 select SF11 to enable the 50 kHz filter and set a 1 second gap between measurements by pressing:

1 SHIFT STORE SAMPLE

(3) Set the AF Source to the frequencies shown in Table 7.12.

TABLE 7.12

AF Sensitivity PVP Accuracy

Frequency	Set Resolution	Allowable Error	Sensitivity (mV RMS)
5 kHz	6 digits	+/-1.3 Hz	18
10 kHz	3 digits	+/-1.3 Hz	18

(4) At each step set the 2101 as follows:

(a) Set the AF source to 25 mV RMS.

(b) Select SF21 (SMOOTH function) and wait for the reading to settle to 4 decimal places.

(c) Press: SHIFT STORE OFFSET SHIFT OFFSET

(d) Select SF20 to disable the SMOOTH function.

(e) Measure the actual sensitivity of the 2101, ensuring that the reading is zero +/- the allowable error.

(f) Press SHIFT OFFSET

(5) Disconnect the test equipment.

Input B Sensitivity PVP

82 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	2
BNC(m)-BNC(m) Coax. Qty 2	18

83 (1) Connect the equipment as shown in Fig. 7.21. Check that the EXT STD indicator is lit.

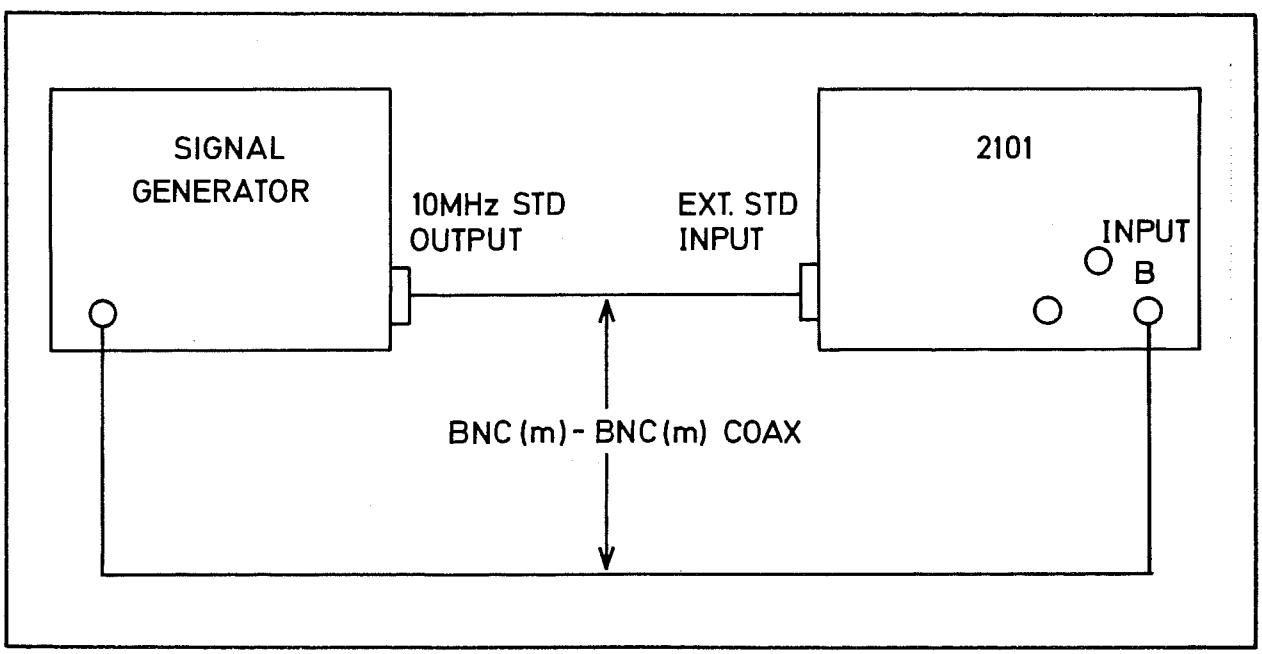


Fig. 7.21 Connection for Input B Sensitivity PVP

(2) Set the signal generator to each of the frequencies shown in Table 7.13 and at each step measure the actual sensitivity of the 2101. Check that the sensitivity is not worse than the figure shown.

(3) Disconnect the equipment.

TABLE 7.13

Input B Sensitivity PVP Accuracy

Frequency (MHz)	Set Resolution	Allowable Error	Sensitivity (mV RMS)
40 MHz	8 digits	+/-1 Hz	8.5
100 MHz	8 digits	+/-2 Hz	8.5
500 MHz	9 digits	+/-1 Hz	8.5
1000 Mhz	9 digits	+/-2 Hz	8.5
1300 Mhz	9 digits	+/-3 Hz	43

Input C Sensitivity PVP

84 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1
Power Meter	5
Precision Power Splitter	13
Precision 20 dB Attenuator	14
3.5(m)-3.5(m) Coax.	17
BNC(m)-BNC(m) Coax. Qty 2	18
N(m)-SMA(m) Adaptor	21 *
N(f)-BNC(f) Adaptor	25
PC3.5(m)-PC3.5(m) Adaptor	35 **

* Not required if Rear Inputs Option 01 is fitted.
** Only required if Rear Inputs Option 01 is fitted.

85 (1) Connect the equipment as shown in Fig. 7.22 (Fig. 7.23 if Rear Inputs Option 01 is fitted).

(2) Set the signal generator to each of the frequencies shown in Table 7.14 and at each step measure the actual sensitivity of the 2101. Check that the sensitivity is not worse than the figure shown.

(3) Disconnect the equipment.

TABLE 7.14

Input C Sensitivity PVP Accuracy

Frequency (GHz)	Set Resolution	Allowable Error	Sensitivity (dBm) 2101	Sensitivity (dBm) 2101 + Opt 11 (Typical)
0.5	1 Hz	+/-2 Hz	-33	-28
5.0	1 Hz	+/-2 Hz	-33	-28
10.0	1 Hz	+/-2 Hz	-33	-28
12.4	1 Hz	+/-2 Hz	-33	-28
18.0	1 Hz	+/-2 Hz	-28	-22.5
20.0	1 Hz	+/-2 Hz	-28	-22.5

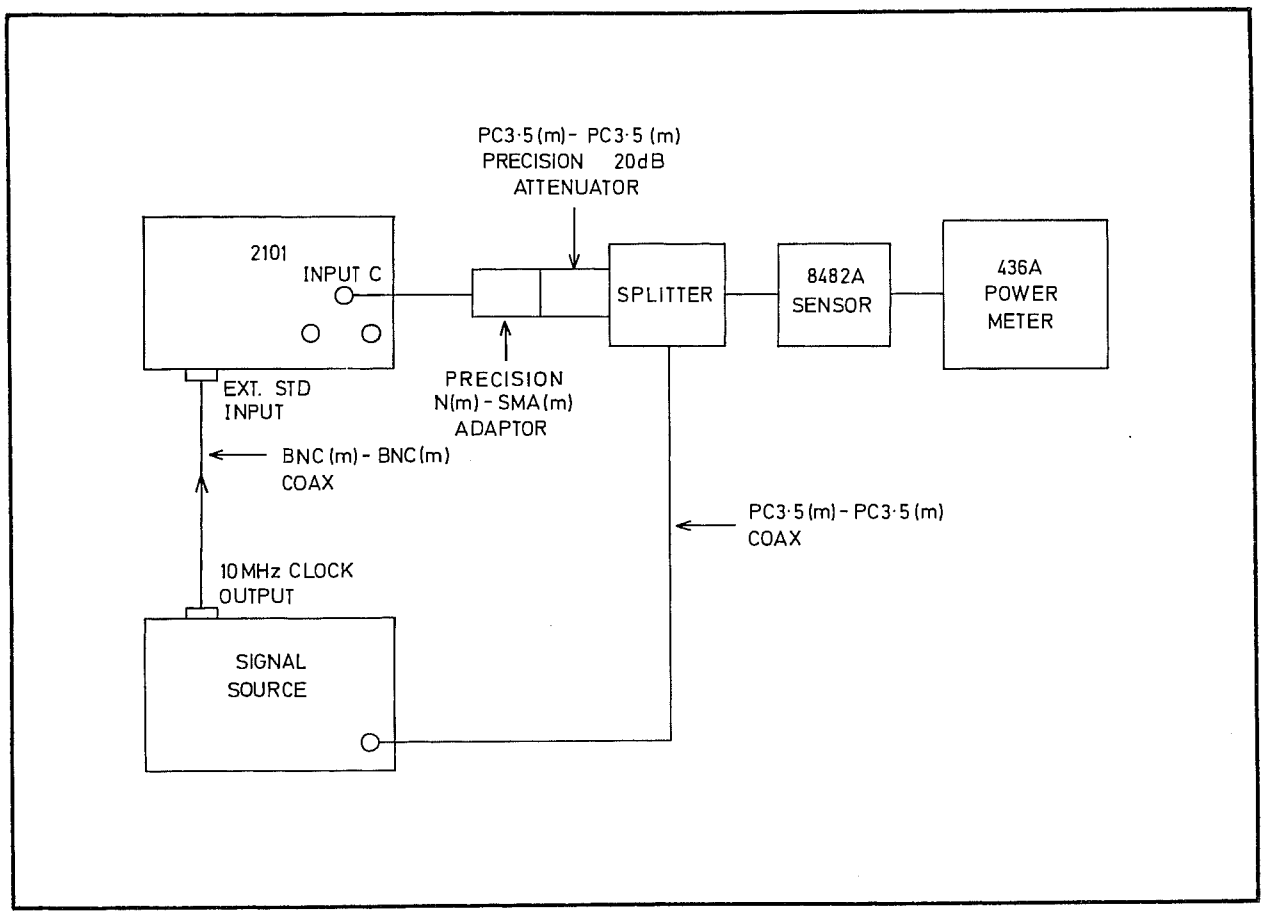


Fig. 7.22 Connections for Channel C Input System PVP

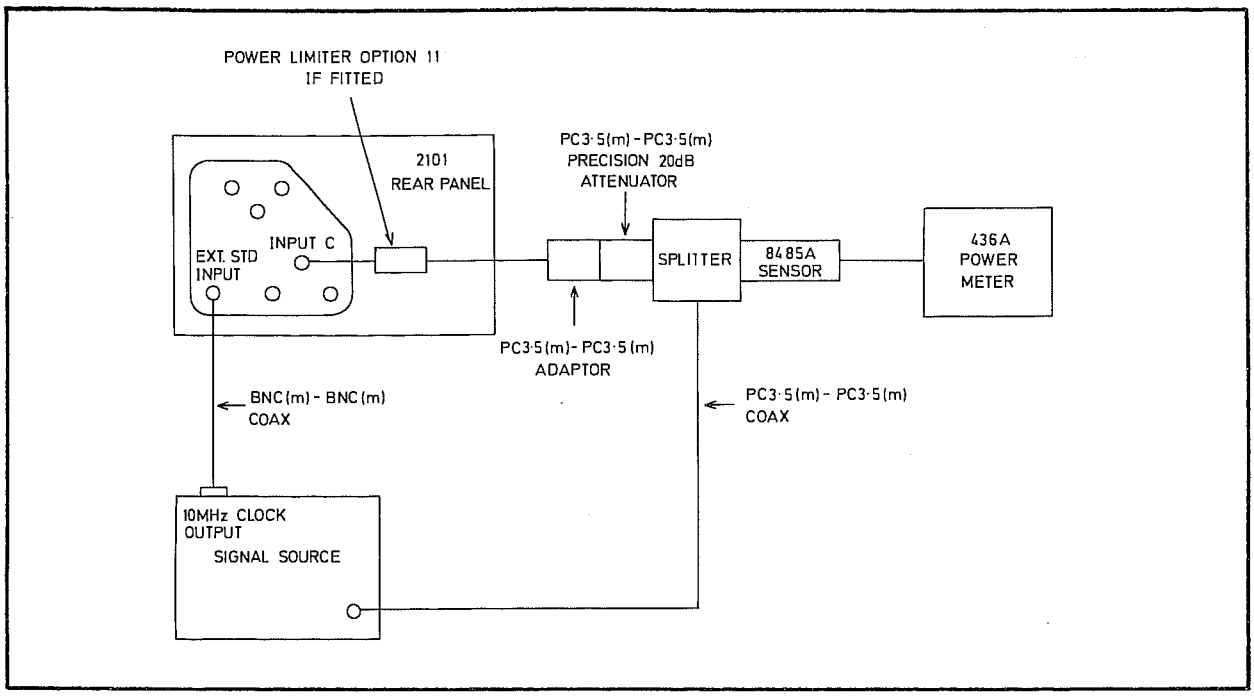


Fig. 7.23 Connections for Channel C Input System PVP with Option 01

External Standard Input Sensitivity PVP

86 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	2
50 Ohms Through Termination	15
BNC(m)-BNC(m) Coax. Qty 2	18

87 (1) Connect the equipment as shown in Fig. 7.24.

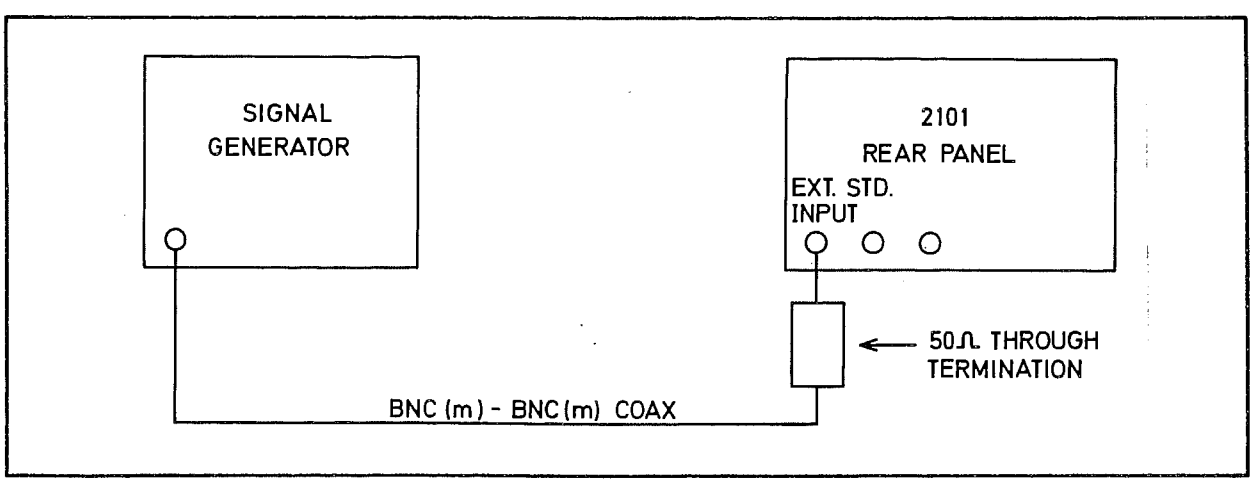


Fig. 7.24 Connection for External Standard Input Sensitivity PVP

(2) Set the signal generator output to 10 MHz at a level of 80 mV RMS.

(3) Verify that the 2101 EXT STD indicator lights steadily.

(4) Disconnect the test equipment.

10 MHz Standard Output Level PVP

88 Test equipment required:

Item	Table 7.1 Item No
Oscilloscope	7
50 Ohms Through Termination	15
BNC(m)-BNC(m) Coax.	18

89 (1) Connect the test equipment as shown in Fig. 7.25.

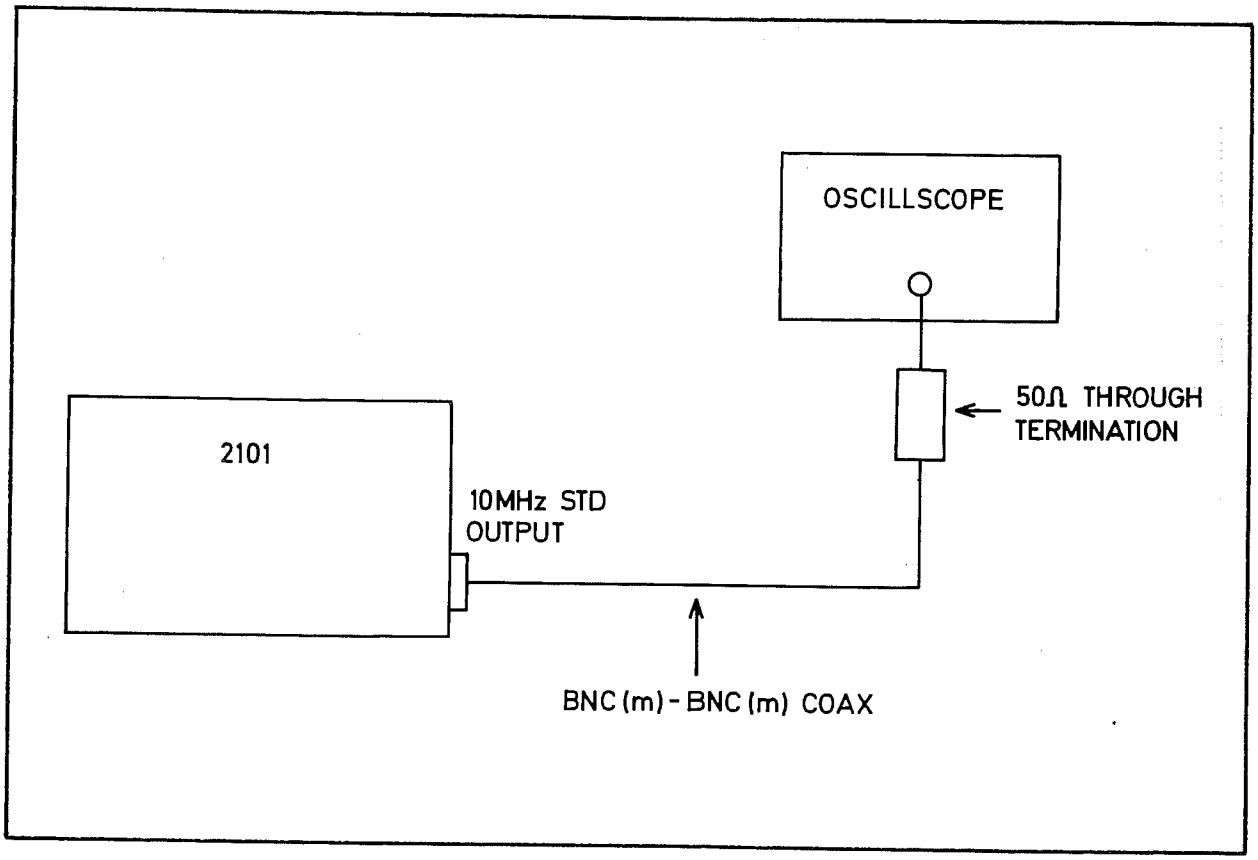


Fig. 7.25 Connection for 10 MHz Standard Output Level PVP

(2) Verify that the peak-to-peak amplitude of the displayed waveform is 1.0 V +/-0.4 V. Verify that the mark/space ratio is between 30:70 and 70:30.

(3) Disconnect the test equipment.

IF Output Level PVP

90 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1
Oscilloscope	7
50 Ohms Through Termination	15
PC3.5(m)-PC3.5(m) Coax.	17
BNC(m)-BNC(m) Coax.	18
N(m)-SMA(f) Adaptor	26 *

* Not required if Rear Inputs Option 01 is fitted.

91 (1) Connect the equipment as shown in Fig. 7.26 (Fig. 7.27 if Option 01 is fitted).

(2) On the 2101 select SF41 and press:

3 4 0 SHIFT MHz TRACK

This sets the LO to 340 MHz. Then set the harmonic number to -37 by pressing:

\- 3 7 SHIFT STORE LOWFM

NOTE: At switch-on the 2101 already has these as default values.

(3) Set the signal generator to 12.5 GHz at -10 dBm and ensure that the 2101 counts correctly.

(4) Verify that the amplitude of the IF is in the range 180 mV to 360 mV peak-to-peak.

(5) Disconnect the test equipment.

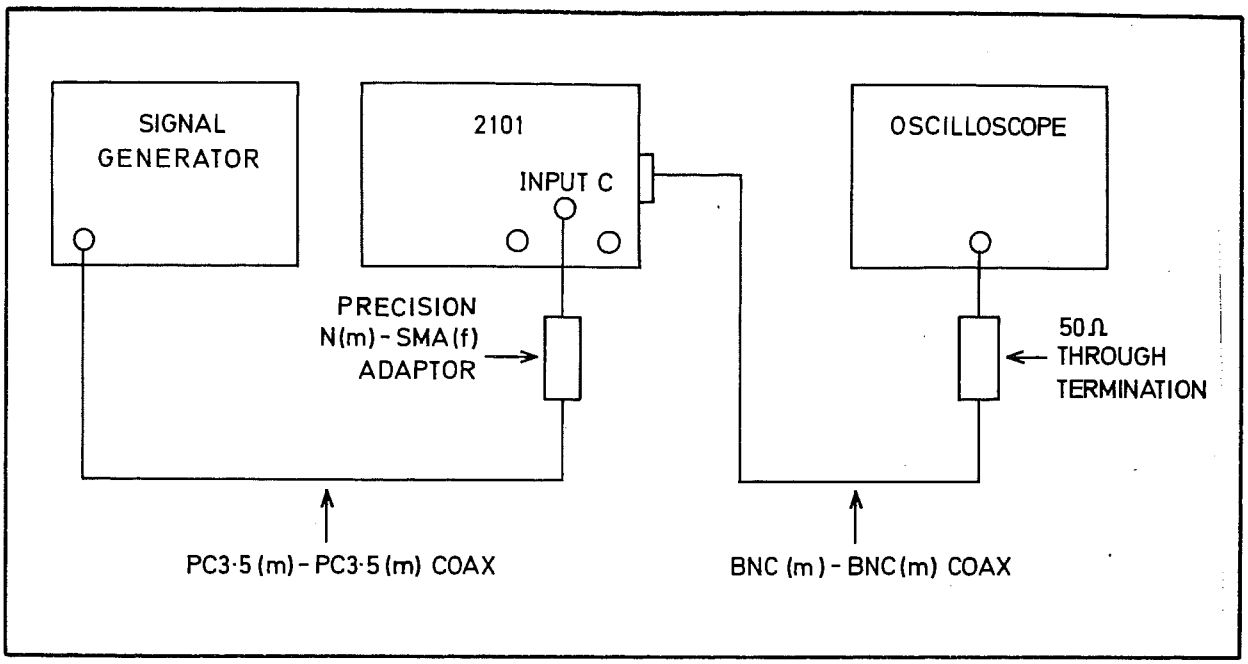


Fig. 7.26 Connection for IF Output Level PVP

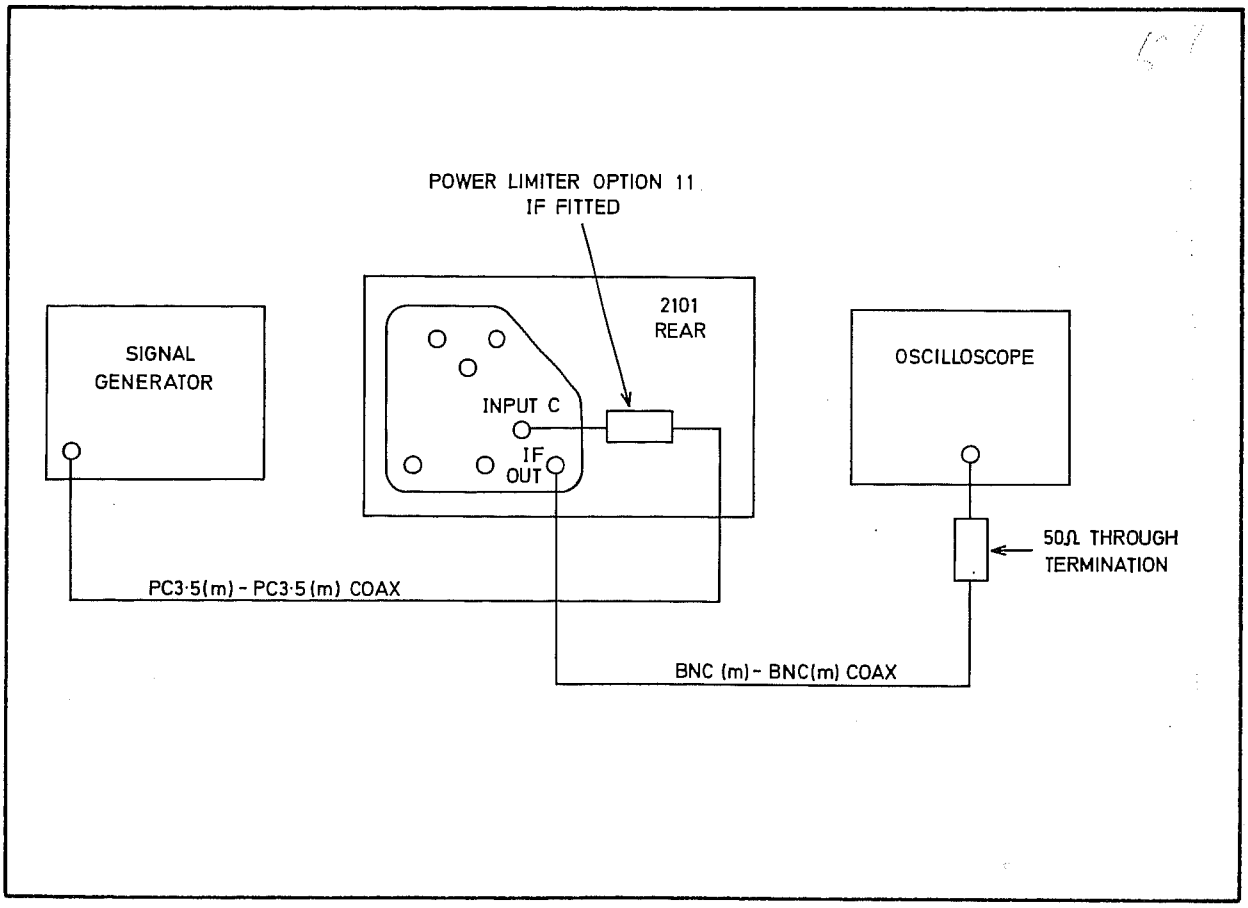


Fig. 7.27 Connection for IF Output Level PVP with Option 01

SECTION 8 PARTS LIST AND CIRCUIT DIAGRAMS

PARTS LIST

CHASSIS ASSEMBLY

(FOR SERVICE SUPPORT)

	Description	Part Number	Qty
FRONT PANEL ASSEMBLY			
Input B	BNC to SMA socket, fused	17-1038	
	Display PCB Assembly	19-3019	
	Front Overlay	13-7004	
	Glue Gasket for Front Overlay	13-6029	
REAR PANEL ASSEMBLY			
	BNC Board Assembly	19-3026	
	Cable Assembly, Co-Axial	10-3529	
LEFT-HAND PANEL ASSEMBLY			
	Fan	23-9175	
MODULE STACK ASSEMBLY			
	IF Module Assembly	11-7049	
	LO Module Assembly	11-7050	
	Mounting Bracket, Right-Hand Side	13-5015	
	Mounting Bracket, Left-Hand Side	13-5016	
	Ribbon Cable Assembly, PL27 - PL34	10-3265	
	Ribbon Cable Assembly, PL28 - PL35	10-3266	
	Co-axial Cable Assembly, PL36 - PL39	10-3527	
	Co-axial Cable Assembly, PL32 - PL33	10-3528	

	Description	Part Number	Qty
ENCLOSURE			
	Top Cover	13-2531	1
	Label for Top Cover inside	15-6022	1
	Adhesive Film	13-6025	1
	Bottom Cover	13-2530	1
	Tilt Bail	15-0675	1
	Foot	24-8700	4
	Strip Rubber Insert for Foot	24-8702	4
	Round Rubber Insert for Foot	24-8704	4
	Screw No.8B x 3/8 inch PLASTITE FLANGE HEAD for Foot	24-5837	4
	Adhesive - Rapid set, for Rubber Inserts	24-6070	

PARTS LIST

BNC MOUNTING BOARD 19-3026

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Connectors					
SK19		Two-way Socket			23-5159
SK20		Two-way Socket			23-5159
SK24		Socket BNC			23-3421
SK26		Socket BNC			23-3421

PARTS LIST

MOTHERBOARD ASSEMBLY 19-3022

Figs 3, 4 and 5

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Resistors					
	Ohms		W		
R1	100	Carbon Film	1	5	20-4651
R2	1M	Carbon Film	0.125	1	20-4995
R3	10k	Chip	0.125	5	20-5768
R4	470	Chip	0.125	5	20-5765
R5	470	Chip	0.125	5	20-5765
R6	150	Chip	0.125	5	20-5783
R7	10k	Potentiometer			20-7071
R8	10k	Chip	0.125	5	20-5768
R9	68	Chip	0.125	5	20-5780
R10	470	Chip	0.125	5	20-5765
R11	10	Chip	0.125	5	20-5771
R12	10	Chip	0.125	5	20-5771
R13	10k	Chip	0.125	5	20-5768
R14	1k	Chip	0.125	5	20-5792
R15	330	Chip	0.125	5	20-5787
R16	330	Chip	0.125	5	20-5787
R17	120	Chip	0.125	5	20-5782
R18	120	Chip	0.125	5	20-5782
R19	330	Chip	0.125	5	20-5787
R20	33	Chip	0.125	5	20-5776
R21	220	Chip	0.125	5	20-5785
R22	68	Chip	0.125	5	20-5780
R23	10k	Chip	0.125	5	20-5768
R24	10	Chip	0.125	5	20-5771
R25	330	Chip	0.125	5	20-5787
R26	330	Chip	0.125	5	20-5787
R27	47	Chip	0.125	5	20-5778
R28	68	Chip	0.125	5	20-5780
R29	10k	SIL x 9			20-5545
R30	330	Chip	0.125	5	20-5787
R31	82	Chip	0.125	5	20-5781
R32	100	Chip	0.125	5	20-5764
R33	47k	Chip	0.125	5	20-5809
R34	100k	Chip	0.125	5	20-5813
R35	4.7k	Chip	0.125	5	20-5799

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
R36	10k	Chip	0.125	5	20-5768
R37	4.7k	Chip	0.125	5	20-5799
R38	10k	Chip	0.125	5	20-5768
R39	2.2k	Chip	0.125	5	20-5796
R40	10k	Chip	0.125	5	20-5768
R41	4.7k	Chip	0.125	5	20-5799
R42	2.2k	Chip	0.125	5	20-5796
R43	4.7k	Chip	0.125	5	20-5799
R44	6.8k	Chip	0.125	5	20-5801
R45	100k	Chip	0.125	5	20-5813
R46	10k	Chip	0.125	5	20-5768
R47	68	Chip	0.125	5	20-5780
R48	10k	Chip	0.125	5	20-5768
R49	10k	Chip	0.125	5	20-5768
R50	10k	Chip	0.125	5	20-5768
R51	10k	Chip	0.125	5	20-5768
R52	100k	Chip	0.125	5	20-5813
R53	1k	Chip	0.125	5	20-5792
R54	330	Chip	0.125	5	20-5787
R55	82	Chip	0.125	5	20-5781
R56	120	Chip	0.125	5	20-5782
R57	10k	Chip	0.125	5	20-5768
R58	10k	Chip	0.125	5	20-5768
R59	10k	Chip	0.125	5	20-5768
R60	1k	Chip	0.125	5	20-5792
R61	10k	Chip	0.125	5	20-5768
R62	10k	Chip	0.125	5	20-5768
R63	4.7k	Chip	0.125	5	20-5799
R64	220	Chip	0.125	5	20-5785
R65	2.2k	Chip	0.125	5	20-5796
R66	470	Chip	0.125	5	20-5765
R67	1.5k	Chip	0.125	5	20-5794
R68	10k	Chip	0.125	5	20-5768
R69	10k	Chip	0.125	5	20-5768
R70	22	Chip	0.125	5	20-5774
R71	10k	Chip	0.125	5	20-5768
R72	10k	Chip	0.125	5	20-5768
R73		Not used			
R74	470	Chip	0.125	5	20-5765
R75	1k	Chip	0.125	5	20-5792

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
R76	1.2k	Chip	0.125	5	20-5793
R77	2k	Potentiometer			20-7030
R78	10k	Chip	0.125	5	20-5768
R79	10k	Chip	0.125	5	20-5768
R80	0	Chip	0.125		20-5870
R81 to R90		Not used			
R91		Not used			
R92	68	Chip	0.125	5	20-5780
R93	10k	Chip	0.125	5	20-5768
R94	1k	Chip	0.125	5	20-5792
R95	470	Chip	0.25	5	20-2471
R96	9.1k	Chip	0.25	1	20-5869
R97	3.9k	Chip	0.125	5	20-5798
R98	10k	SIL x 5			20-5562
R99	1k	Chip	0.125	5	20-5792
R100	100	Chip	0.25	5	20-2101
R101	1k	Chip	0.125	5	20-5792
R102	10k	Chip	0.125	5	20-5768
R103	47	Chip	0.5	5	20-3470
R104		SIL			20-5556
R105		Not used			
R106	100	Chip	0.25	5	20-2101
R107	1k	Chip	0.125	5	20-5792
R108	4.7k	Chip	0.125	5	20-5799
R109	18	Chip	0.125	5	20-5763
R110	68	Chip	0.125	5	20-5780
R111		Not used			
R112	82	Chip	0.125	5	20-5781
R113	82	Chip	0.125	5	20-5781
R114	10	Chip	0.125	5	20-5771
R115	27	Chip	0.125	5	20-5775
R116		Not used			
R117		Not used			
R118	4.7k	Chip	0.125	5	20-5799
R119	10k	Chip	0.125	5	20-5768
R120		Not used			

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
R121	220	Chip	0.125	5	20-5785
R122	4.7k	Chip	0.125	5	20-5799
R123	2.2	Chip	0.125	5	20-5796
R124	10k	Chip	0.125	5	20-5786
R125	330	Chip	0.125	5	20-5787
R126	1k	Chip	0.125	5	20-5792
R127	1k	Chip	0.125	5	20-5792
R128	3.3k	Chip	0.125	5	20-5797
R129	1k	Chip	0.125	5	20-5792
R130	100k	Chip	0.125	5	20-5813
R131	3.3k	Chip	0.125	5	20-5797
R132	1k	Chip	0.125	5	20-5792
R133		Not used			
R134	470	Chip	0.125	5	20-5765
R135	1k	Chip	0.125	5	20-5792
R136	470	Chip	0.125	5	20-5765
R137	1k	Chip	0.125	5	20-5792
R138	1k	Chip	0.125	5	20-5792
R139	10k	Chip	0.125	5	20-5768
R140	100k	Chip	0.125	5	20-5813
R141	1k	Chip	0.125	5	20-5792
R142	1k	Chip	0.125	5	20-5792
R143	1k	Chip	0.125	5	20-5792
R144	1k	Chip	0.125	5	20-5792
R145	1k	Chip	0.125	5	20-5792
R146	3.3k	Chip	0.125	5	20-5797
R147	1k	Chip	0.125	5	20-5792
R148	100k	Chip	0.125	5	20-5813
R149	100k	Chip	0.125	5	20-5813
R150	100k	Chip	0.125	5	20-5813
R151	68k	Chip	0.125	5	20-5811
R152	100k	Chip	0.125	5	20-5813
R153	1k	Chip	0.125	5	20-5792
R154	10k	Chip	0.125	5	20-5768
R155	1k	Chip	0.125	5	20-5792
R156	100	Chip	0.25	5	20-2101
R157	10M	Chip	0.125	5	20-5867
R158	10k	Chip	0.125	5	20-5768
R159	10k	Chip	0.125	5	20-5768
R160	220	Chip	0.125	5	20-5785

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Capacitors					
	F		V		
C1	20n	Chip Ceramic	400	10	21-1847
C2	10n	Chip Ceramic	50	20	21-1801
C3	10n	Chip Ceramic	50	20	21-1801
C4	100u	Electrolytic	10	20	21-0678
C5	100u	Electrolytic	10	20	21-0678
C6	10n	Chip Ceramic	50	20	21-1801
C7	47u	Electrolytic	25	20	21-0789
C8	10n	Chip Ceramic	50	20	21-1801
C9	47u	Electrolytic	25	20	21-0789
C10	10n	Chip Ceramic	50	20	21-1801
C11	10n	Chip Ceramic	50	20	21-1801
C12	10n	Chip Ceramic	50	20	21-1801
C13	10n	Chip Ceramic	50	20	21-1801
C14	10n	Chip Ceramic	50	20	21-1801
C15	47u	Electrolytic	25	20	21-0789
C16	10n	Chip Ceramic	50	20	21-1801
C17	33n	Chip Ceramic	50	10	21-1808
C18	10n	Chip Ceramic	50	20	21-1801
C19	47u	Electrolytic	25	20	21-0789
C20	10n	Chip Ceramic	50	20	21-1801
C21	47u	Electrolytic	25	20	21-0789
C22	1n	Chip Ceramic	50	20	21-1800
C23	10n	Chip Ceramic	50	20	21-1801
C24	100p	Chip Ceramic	50	5	21-1798
C25	1n	Chip Ceramic	50	20	21-1800
C26	10n	Chip Ceramic	50	20	21-1801
C27	1u	Electrolytic	50	20	21-0779
C28	1n	Chip Ceramic	50	20	21-1800
C29	33n	Chip Ceramic	50	10	21-1808
C30	47u	Electrolytic	25	20	21-0789
C31	1u	Electrolytic	50	20	21-0779
C32	33n	Chip Ceramic	50	10	21-1808
C33	33n	Chip Ceramic	50	10	21-1808
C34	10u	Electrolytic	16	20	21-0775
C35	10n	Chip Ceramic	50	20	21-1801

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
C36	33n	Chip Ceramic	50	10	21-1808
C37	10n	Chip Ceramic	50	20	21-1801
C38	33n	Chip Ceramic	50	10	21-1808
C39	33n	Chip Ceramic	50	10	21-1808
C40	47u	Electrolytic	25	20	21-0789
C41	10n	Chip Ceramic	50	20	21-1801
C42	10n	Chip Ceramic	50	20	21-1801
C43	470u	Electrolytic	40	20	21-0688
C44	10n	Chip Ceramic	50	20	21-1801
C45	10n	Chip Ceramic	50	20	21-1801
C46	330u	Electrolytic	10	-10/+50	21-0618
C47		Not used			
C48	120p	Chip Ceramic	50	5	21-1845
C49	47u	Electrolytic	25	20	21-0789
C50	120p	Chip Ceramic	50	5	21-1845
C51	47u	Electrolytic	25	20	21-0789
C52	120p	Chip Ceramic	50	5	21-1845
C53	1u	Electrolytic	50	20	21-0779
C54	47u	Electrolytic	25	20	21-0789
C55	1u	Electrolytic	50	20	21-0779
C56	120p	Chip Ceramic	50	5	21-1845
C57	47u	Electrolytic	25	20	21-0789
C58	33n	Chip Ceramic	50	10	21-1808
C59	33n	Chip Ceramic	50	10	21-1808
C60	22000u	Electrolytic	16		21-0806
C61	4700u	Electrolytic	16	-10/+30	21-0667
C62	1000u	Electrolytic	35	20	21-0800
C63	10n	Chip Ceramic	50	20	21-1801
C64	10n	Chip Ceramic	50	20	21-1801
C65		Not used			
C66	15p	Chip Ceramic	50	5	21-1789
C67	27p	Chip Ceramic	50	5	21-1792
C68	4.7u	Electrolytic	63		21-0750
C69	10n	Chip Ceramic	50	20	21-1801
C70	100p	Chip Ceramic	50	5	21-1798
C71	20n	Chip Ceramic	400	10	21-1847
C72	1n	Chip Ceramic	50	20	21-1800
C73	33n	Chip Ceramic	50	10	21-1808
C74	10n	Chip Ceramic	50	20	21-1801
C75	10n	Chip Ceramic	50	20	21-1801

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
C76	1n	Chip Ceramic	50	20	21-1800
C77	100p	Chip Ceramic	50	5	21-1798
C78	10n	Chip Ceramic	50	20	21-1801
C79	1n	Chip Ceramic	50	20	21-1800
C80	100p	Chip Ceramic	50	5	21-1798
C81	47u	Electrolytic	25	20	21-0789
C82	10n	Chip Ceramic	50	20	21-1801
C83	10n	Chip Ceramic	50	20	21-1801
C84		Not used			
C85	47u	Electrolytic	25	20	21-0789
C86	10n	Chip Ceramic	50	20	21-1801
C87	1n	Chip Ceramic	50	20	21-1800
C88	100p	Chip Ceramic	50	5	21-1798
C89	4.7u	Electrolytic	63		21-0750
C90	4.7u	Electrolytic	63		21-0750
C91	4.7u	Electrolytic	63		21-0750
C92	4.7u	Electrolytic	63		21-0750
C93	100p	Chip Ceramic	50	5	21-1798
C94	4.7u	Electrolytic	63		21-0750
C95	120p	Chip Ceramic	50	5	21-1845
C96	47u	Electrolytic	25	20	21-0789
C97	47u	Electrolytic	25	20	21-0789
C98	10n	Chip Ceramic	50	20	21-1801

Diodes

D1	Dual Diode BAV99	22-1096
D2	Dual Diode BAV99	22-1096
D3	Dual Diode BAW56	22-1094
D4	Silicon BAS16	22-1093
D5	Dual Diode BAV99	22-1096
D6	Dual Diode BAV99	22-1096
D7	Dual Diode BAV99	22-1096
D8	Dual Diode BAW56	22-1094
D9	Zener BZX79B5V1	22-1857
D10	Not used	

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
D11		Rectifier			22-1662
D12		Rectifier			22-1662
D13		Silicon BAS16			22-1093
D14		Dual Diode BAV99			22-1096
D15		Dual Diode BAW56			22-1094
D16		Zener BZX79B5V1			22-1857
Transistors					
Q1		BF256A			22-6163
Q2		BFS17			22-6206
Q3		CA3083			22-4216
Q4		BSR18A			22-6199
Q5		BSR18A			22-6199
Q6		BSR17A			22-6197
Q7		BSR17A			22-6197
Q8		BSR18A			22-6199
Q9		ZTX550			22-6113
Q10		BSR18A			22-6199
Q11		BDT92			22-6153
Q12		BSR17A			22-6197
Q13		BDT92			22-6153
Q14		BSR17A			22-6197
Q15		BDT92			22-6153
Q16		BSR17A			22-6197
Q17		BSR17A			22-6197
Q18		BSR18A			22-6199
Q19		BDT91			22-6152
Q20		BDT92			22-6153
Q21		BSR17A			22-6197
Q22		BSR17A			22-6197
Integrated Circuits					
IC1		MC10116			22-4528
IC2		LM339			22-4249
IC3		MC3403			22-4262
IC4		MC10116			22-4528
IC5		6116			22-8206

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
IC6		MC146805E2			22-8307
IC7		MCC1			22-8403
IC8		MCC2			22-8404
IC9		MC10231			22-4542
IC10		27256			22-8592
IC11		78L12AC			22-4321
IC12		74LS138			22-4587
IC13		74HGT373			22-4808
IC14		74HGT373			22-4808
IC15		74LS138			22-4587
IC16		74HCT00			22-4800
IC17		74LS04			22-4533
IC18		74LS373			22-4585
IC19		74LS10			22-4557
IC20		74LS32			22-4578
IC21		74LS74			22-4534
IC22		74LS244			22-4807
IC23		40106			22-4756
IC24		4011			22-4700
IC25		SP9687DG			22-4686
IC26		uA741			22-4111
IC27		74LS244			22-4807
Inductors					
	H				
L1	1u	Coil		10	23-7192
L2	10u	Coil		10	23-7155
L3	100u	Coil		10	23-7213
L4	100u	Coil		10	23-7213
L5	100u	Coil		10	23-7213
L6	100u	Filter Coil		15	23-7223
L7	100u	Filter Coil		15	23-7223
Transformers					
T1		Mains Transformer			17-4152

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Connectors					
PL1		Plug 2 x 7-Way			23-5162
PL2		Plug 2 x 7-Way			23-5162
PL7		Plug 30-Way			23-5174
PL10		Connector, Mains filtered			23-3420
PL14		Plug 5-Way			23-5164
PL15		Connector 8-Way			23-5190
PL16		Plug 10-Way			23-5165
PL17		Plug 5-Way			23-5164
PL19		Plug 2 x 2-Way			23-5161
PL20		Plug 2 x 2-Way			23-5161
PL21		Plug 2 x 12-Way			23-5197
PL27		Plug, right-angle 20-Way			23-3484
PL28		Plug, right-angle 20-Way			23-3484
PL30		Connector Assembly			10-3531
PL31		Header 2 x 4-Way			23-5661
PL37		Connector Assembly			10-3530
PL38		Plug SMB right-angle			23-3338
SK4		IC Socket 28-Way DIL			23-3290
SK5		Socket BNC			17-1043
		Mains Socket Assembly			11-4005
Miscellaneous					
FS2		Fuse Link			23-0032
H1		Hybrid TEC			17-1034
LK1		Link			23-5180
RL1		Relay			23-7530
S1		Mains Switch			23-4124
XL1		Crystal 5MHz			23-9176

PARTS LIST

DISPLAY ASSEMBLY 19-3019

Fig. 7

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Resistors					
	Ohms		W		
R1	10k	Carbon Film	0.25	5	20-2103
R2	10k	Carbon Film	0.25	5	20-2103
R3	10k	SIL x 9			20-5521
Capacitors					
	F		V		
C1	100n	Ceramic	50	20	21-1708
C2	4.7u	Electrolytic	50	20	21-0750
C3	100n	Ceramic	50	20	21-1708
C4	100n	Ceramic	50	20	21-1708
C5	100n	Ceramic	50	20	21-1708
Diodes					
D1		1N4149			22-1029
DI1		Display, double digit			26-1512
DI2		Display, double digit			26-1512
DI3		Display, double digit			26-1512
DI4		Display, double digit			26-1512
DI5		Display, double digit			26-1512
DI6		Display, double digit			26-1512
DI7		Display, single digit			26-1513
LP1-28		LED			26-5026
Integrated Circuits					
IC1		4012			22-4754
IC2		MM74C922N			22-4779
IC3		7218AIJI			22-4778
IC4		7218AIJI			22-4778

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Connectors					
SK1		Socket 14-Way			23-5160
SK2		Socket 14-Way			23-5160
SK4		IC Socket 28-Way DIL (IC4)			23-3290
Switches					
S1-19		Switch			23-4125
		Button, Grey			15-0703
		Button, Blue			15-0705
		Button, No. 1			15-0651
		Button, No. 2			15-0652
		Button, No. 3			15-0653
		Button, No. 4			15-0654
		Button, No. 5			15-0655
		Button, No. 6 or 9			15-0656
		Button, No. 7			15-0657
		Button, No. 8			15-0658
		Button, No. 0			15-0659
		Button, Decimal Point	15-0660		

PARTS LIST

GPIB ASSEMBLY 19-1146

Fig. 9

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Resistors					
	Ohms		W		
R1	9x3.3k	SIL Array			20-5532
R2	56	Carbon Film	0.25	5	20-2560
R3	10k	SIL Array			20-5532
R4	330	Carbon Film	0.25	5	20-2331
R5	330	Carbon Film	0.25	5	20-2331
R6	330	Carbon Film	0.25	5	20-2331
R7	5x3.3k	SIL Array			20.5531
R8	18	Carbon Film	0.25	5	20-2180
R9	56	Carbon Film	0.25	5	20-2560
R10	9x100k	SIL Array			20-5522
R11	5x100k	SIL Array			20-5558
Capacitors					
	F		V		
C1	47u	Electrolytic	25	20	21-0789
C2	100n	Ceramic	50	20	21-1708
C3	100n	Ceramic	50	20	21-1708
C4	100n	Ceramic	50	20	21-1708
C5	100n	Ceramic	50	20	21-1708
C6	100n	Ceramic	50	20	21-1708
C7	100n	Ceramic	50	20	21-1708
C8	100n	Ceramic	50	20	21-1708
C9	10n	Ceramic	25	-20+80	21-1545
C10	10n	Ceramic	25	-20+80	21-1545
Integrated Circuits					
IC1		74HCT374			22-4809
IC2		74HCT374			22-4809
IC3		74HCT138			22-4806
IC4		7407			22-4063
IC5		74LS125			22-4657

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
IC6		74HCT02			22-4801
IC7		74HCT00			22-4800
IC8		74HCT138			22-4806
IC9		MC14805			22-8307
IC10		Programmed ROM			22-8597

NOTE: When ordering a replacement for IC10, it is essential that the software issue number and the serial number of the instrument are quoted in addition to the part number. The software issue number is marked on the component.

IC11		74HCT373			22-4808
IC12		68488			22-8305
IC13		4066			22-4761
IC14		75161			22-4284
IC15		75160			22-4283
IC16		74HCT74			22-4805
IC17		74HCT74			22-4805
IC18		74HCT00			22-4800
IC19		74HCT02			22-4801
IC20		74HCT32			22-4804

Miscellaneous

		IC Socket, 28-way			23-3290
		IC Socket, 40-way			23-3297
		IC Socket, 14-way			23-3309
SK3		Connector, 24-way			23-3434
s1		Switch, 6-way, DIL			23-4102

PARTS LIST

PRESCALER ASSEMBLY 19-3052

Figs 11 and 12

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Resistors	Ohms		W		
R1		Not used			
R2		Not used			
R3	10k	Chip	0.125	5	20-5768
R4	10k	Chip	0.125	5	20-5768
R5	150	Chip	1		20-5841
R6	39	Chip	1		20-5837
R7	330	Chip	0.125	5	20-5787
R8	150	Chip	0.125	5	20-5783
R9	270	Chip	0.125	5	20-5786
R10	100	Chip	0.125	5	20-5764
R11	270	Chip	0.125	5	20-5786
R12	10	Chip	0.125	5	20-5771
R13	33	Chip	0.125	5	20-5776
R14	330	Chip	0.125	5	20-5787
R15	270	Chip	0.125	5	20-5786
R16	390	Chip	0.125	5	20-5788
R17		Not used			
R18	10	Chip	0.125	5	20-5771
R19	33	Chip	0.125	5	20-5776
R20	330	Chip	0.125	5	20-5787
R21	180	Chip	0.125	5	20-5784
R22	180	Chip	0.125	5	20-5784
R23	390	Chip	0.125	5	20-5788
R24	10	Chip	0.125	5	20-5771
R25	33	Chip	0.125	5	20-5776
R26	330	Chip	0.125	5	20-5787
R27	20k	Potentiometer			20-7049
R28	390	Chip	0.125	5	20-5788
R29	100k	Chip	0.125	5	20-5813
R30	30	Chip	0.125	5	20-5771
R31	22	Chip	0.125	5	20-5774
R32	220	Chip	0.125	5	20-5785
R33	1.5k	Chip	0.125	5	20-5794
R34	1.5k	Chip	0.125	5	20-5794
R35	56k	Chip	0.125	5	20-5810

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
R36	10	Chip	0.125	5	20-5771
R37	56	Chip	0.125	5	20-5779
R38	56k	Chip	0.125	5	20-5810
R39	1M	Chip	0.125	5	20-5770
R40		Not used			
R41	4.7k	Chip	0.125	5	20-5799
R42	4.7k	Chip	0.125	5	20-5799
R43		Not used			
R44	1k	Chip	0.125	5	20-5792
R45	150	Chip	0.125	5	20-5783
R46	27	Chip	0.125	5	20-5775
R47	27	Chip	0.125	5	20-5775
R48	27	Chip	0.125	5	20-5775
R49	27	Chip	0.125	5	20-5775
R50	470	Chip	0.125	5	20-5765
R51		Not used			
R52	6.8k	Chip	0.125	5	20-5801
R53	3.3k	Chip	0.125	5	20-5797
R54	1k	Chip	0.125	5	20-5792
R55	1k	Chip	0.125	5	20-5792
R56	680	Chip	0.125	5	20-5790
R57	2.7k	Chip	0.125	5	20-5766
R58	3.3k	Chip	0.125	5	20-5797
R59	1k	Chip	0.125	5	20-5792
R60	1k	Chip	0.125	5	20-5792
R61	1k	Chip	0.125	5	20-5792
R62	1k	Chip	0.125	5	20-5792
R63		Not used			
R64		Not used			
R65		Not used			
R66	150	Chip	0.125	5	20-5783
R67		Not used			
R68	1M	Chip	0.125	5	20-5770
R69	1M	Chip	0.125	5	20-5770
R70	10	Chip	0.125	5	20-5771
R71	10	Chip	0.125	5	20-5771

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Capacitors					
	F		V		
C1	10n	Chip			21-1801
C2	10n	Chip			21-1801
C3	10n	Chip			21-1801
C4	10n	Chip			21-1801
C5	10n	Chip			21-1801
C6	10n	Chip			21-1801
C7	3.3p	Chip			21-1781
C8	10n	Chip			21-1801
C9	10n	Chip			21-1801
C10	10n	Chip			21-1801
C11	3.3p	Chip			21-1781
C12	10n	Chip			21-1801
C13	10n	Chip			21-1801
C14	3.3p	Chip			21-1781
C15	10n	Chip			21-1801
C16	47u	Electrolytic			21-0615
C17	10n	Chip			21-1801
C18	10n	Chip			21-1801
C19	4.7p	Chip			21-1783
C20		Not used			
C21	4.7p	Chip			21-1783
C22	3.3p	Chip			21-1781
C23	12p	Chip			21-1788
C24	10n	Chip			21-1801
C25	10n	Chip			21-1801
C26	1n	Chip			21-1800
C27	47u	Chip			21-0615
C28	10n	Chip			21-1801
C29	10n	Chip			21-1801
C30	10n	Chip			21-1801
C31	10n	Chip			21-1801
C32	10n	Chip			21-1801
C33	5.6p	Chip			21-1784
C34	6.8p	Chip			21-1785
C35	6.8p	Chip			21-1785

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
C36	6.8p	Chip			21-1785
C37	47p	Chip			21-1795
C38	10n	Chip			21-1801
C39	10n	Chip			21-1801
C40	3.3p	Chip			21-1781
C41	3.3p	Chip			21-1781
C42	5.6p	Chip			21-1784
C43	10n	Chip			21-1801
C44	47u	Electrolytic			21-0615
C45	47u	Electrolytic			21-0615
C46	3.9p	Chip			21-1782
C47	10n	Chip			21-1801
C48	10n	Chip			21-1801
C49	3.3p	Chip			21-1781
C50	3.3p	Chip			21-1781
C51	15p	Chip			21-1789
C52	15p	Chip			21-1789
C53	100n	Chip			21-1708
Diodes					
D1		5082-2835			22-1086
D2		5082-3379			22-1058
D3		5082-2835			22-1086
D4		Not used			
D5		5082-2835			22-1086
D6		5082-2835			22-1086
D7		5082-3379			22-1058
D8		5082-2800			22-1068
D9		5082-2800			22-1068
D10		BZX79C9V1			22-1814
D11		BZX79C9V1			22-1814
D12		1N4149			22-1029

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Transistors					
Q1		BFR90			22-6123
Q2		BFR90			22-6123
Q3		BFR90			22-6123
Q4		HXTR3101			22-6155
Integrated Circuits					
IC1		LM339			22-4249
IC2		MC10116			22-4528
IC3		SP4731DP			22-4694
IC4		74LS00			22-4531
Inductors					
L1		Coil Assembly			17-3240
Connectors					
SK7		Connector 30-Way Coaxial Assembly			23-5173 10-3532

PARTS LIST

I.F. PROCESSOR ASSEMBLY 19-3024

Fig. 14

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Resistors					
	Ohms		W		
R1	3.3k	Chip	0.125	5	20-5797
R2	15k	Chip	0.125	5	20-5803
R3	100	Chip	0.125	5	20-5764
R4	150	Chip	0.125	5	20-5783
R5	330	Chip	0.125	5	20-5787
R6	820	Chip	0.125	5	20-5791
R7	1.8k	Chip	0.125	5	20-5795
R8	150	Chip	0.125	5	20-5783
R9	10	Chip	0.125	5	20-5771
R10	15	Chip	0.125	5	20-5773
R11	0	Chip	0.125		20-5870
R12	1.5k	Chip	0.125	5	20-5794
R13	150	Chip	0.125	5	20-5783
R14	50	Potentiometer			20-7127
R15	33	Chip	0.125	5	20-5776
R16	33	Chip	0.125	5	20-5776
R17	47	Chip	0.125	5	20-5778
R18	220	Chip	0.125	5	20-5785
R19	470	Chip	0.125	5	20-5765
R20	470	Chip	0.125	5	20-5765
R21	10	Chip	0.125	5	20-5771
R22	150	Chip	0.125	5	20-5783
R23	680	Chip	0.125	5	20-5790
R24	10	Chip	0.125	5	20-5771
R25	150	Chip	0.125	5	20-5783
R26	470	Chip	0.125	5	20-5765
R27	680	Chip	0.125	5	20-5790
R28	10	Chip	0.125	5	20-5771
R29	220	Chip	0.125	5	20-5785
R30	56	Chip	0.125	5	20-5779
R31	33	Chip	0.125	5	20-5776
R32	470	Chip	0.125	5	20-5765
R33	10	Chip	0.125	5	20-5771
R34	56	Chip	0.125	5	20-5779
R35	0	Chip	0.125		20-5870

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
R36	22k	Chip	0.125	5	20-5805
R37	56	Chip	0.125	5	20-5779
R38	10k	Chip	0.125	5	20-5768
R39	33	Chip	0.125	5	20-5776
R40	10k	Chip	0.125	5	20-5768
R41	47	Chip	0.125	5	20-5778
R42	220	Chip	0.125	5	20-5785
R43	470	Chip	0.125	5	20-5765
R44	4.7k	Chip	0.125	5	20-5799
R45	470	Chip	0.125	5	20-5765
R46	10	Chip	0.125	5	20-5771
R47	150	Chip	0.125	5	20-5783
R48	680	Chip	0.125	5	20-5790
R49	10	Chip	0.125	5	20-5771
R50	150	Chip	0.125	5	20-5783
R51	470	Chip	0.125	5	20-5765
R52	680	Chip	0.125	5	20-5790
R53	10	Chip	0.125	5	20-5771
R54	220	Chip	0.125	5	20-5785
R55	33	Chip	0.125	5	20-5776
R56	470	Chip	0.125	5	20-5765
R57	56	Chip	0.125	5	20-5779
R58	0	Chip	0.125		20-5870
R59	56	Chip	0.125	5	20-5779
R60	33	Chip	0.125	5	20-5776
R61	56	Chip	0.125	5	20-5779
R62	56	Chip	0.125	5	20-5779
R63	390	Chip	0.125	5	20-5788
R64	18	Chip	0.125	5	20-5763
R65	56	Chip	0.125	5	20-5779
R66	10k	Chip	0.125	5	20-5768
R67	1.5k	Chip	0.125	5	20-5794
R68	2.7k	Chip	0.125	5	20-5766
R69	39k	Chip	0.125	5	20-5808
R70	50k	Chip	0.125	5	20-7138
R71	47k	Chip	0.125	5	20-5809
R72	47k	Chip	0.125	5	20-5809
R73	1.5k	Chip	0.125	5	20-5794
R74	1M	Chip	0.125	5	20-5770
R75	10k	Chip	0.125	5	20-5768

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
R76	10k	Chip	0.125	5	20-5768
R77	47k	Chip	0.125	5	20-5809
Capacitors					
	F		V		
C1	6.8u	Chip Electrolytic	25	-10/+50	21-0907
C2	6.8u	Chip Electrolytic	25	-10/+50	21-0907
C3	33n	Chip Ceramic	50	10	21-1808
C4	33n	Chip Ceramic	50	10	21-1808
C5	10n	Chip Ceramic	50	10	21-1801
C6	33n	Chip Ceramic	50	10	21-1808
C7	68p	Chip Ceramic	50	5	21-1797
C8	15u	Chip Electrolytic	10	-10/+50	21-0903
C9	33n	Chip Ceramic	50	10	21-1808
C10	27p	Chip Ceramic	50	5	21-1792
C11	4.7p	Chip Ceramic		+/-0.25p	21-1783
C12	33p	Chip Ceramic	50	5	21-1793
C13	3-10p	Trimmer			21-6046
C14	12	Chip Ceramic	50	5	21-1788
C15	18	Chip Ceramic	50	5	21-1790
C16	1n	Chip Ceramic	50	10	21-1800
C17	1n	Chip Ceramic	50	10	21-1800
C18	10n	Chip Ceramic	50	10	21-1801
C19	100p	Chip Ceramic	50	5	21-1798
C20	10n	Chip Ceramic	50	10	21-1801
C21	33n	Chip Ceramic	50	10	21-1808
C22	33n	Chip Ceramic	50	10	21-1808
C23	68p	Chip Ceramic	50	5	21-1797
C24	10n	Chip Ceramic	50	10	21-1801
C25	10n	Chip Ceramic	50	10	21-1801
C26	100p	Chip Ceramic	50	5	21-1798
C27	33n	Chip Ceramic	50	10	21-1808
C28	10n	Chip Ceramic	50	10	21-1801
C29	10n	Chip Ceramic	50	10	21-1801
C30	10n	Chip Ceramic	50	10	21-1801
C31	27p	Chip Ceramic	50	5	21-1792
C32	100p	Chip Ceramic	50	5	21-1798
C33	39p	Chip Ceramic	50	5	21-1794
C34	27	Chip Ceramic	50	5	21-1792
C35	15u	Chip Electrolytic	10	-10/+50	21-0903

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
C36	15u	Chip Electrolytic	10	-10/+50	21-0903
C37	15u	Chip Electrolytic	10	-10/+50	21-0903
C38	10n	Chip Ceramic	50	10	21-1801
C39	100p	Chip Ceramic	50	5	21-1798
C40	10n	Chip Ceramic	50	10	21-1801
C41	33n	Chip Ceramic	50	10	21-1808
C42	33n	Chip Ceramic	50	10	21-1808
C43	68p	Chip Ceramic	50	10	21-1797
C44	10n	Chip Ceramic	50	10	21-1801
C45	100p	Chip Ceramic	50	5	21-1798
C46	33n	Chip Ceramic	50	10	21-1808
C47	10n	Chip Ceramic	50	10	21-1801
C48	10n	Chip Ceramic	50	10	21-1801
C49	10n	Chip Ceramic	50	10	21-1801
C50	10n	Chip Ceramic	50	10	21-1801
C51	1n	Chip Ceramic	50	10	21-1800
C52	100p	Chip Ceramic	50	5	21-1798
C53	1n	Chip Ceramic	50	10	21-1800
C54	1n	Chip Ceramic	50	10	21-1800
C55	68p	Chip Ceramic	50	5	21-1797
C56	1n	Chip Ceramic	50	10	21-1800
C57	68p	Chip Ceramic	50	5	21-1797
C58	39p	Chip Ceramic	50	5	21-1794
C59	8.2p	Chip Ceramic	50	+/-0.25p	21-1786
C60	47p	Chip Ceramic	50	5	21-1795
C61		Not used			
C62)	18p	Chip Ceramic	50	5	21-1790
Select)	22p	Chip Ceramic	50	5	21-1791
on test)	27p	Chip Ceramic	50	5	21-1792
C63	27p	Chip Ceramic	50	5	21-1792
C64	1n	Chip Ceramic	50	10	21-1800
C65	1n	Chip Ceramic	50	10	21-1800
C66	1n	Chip Ceramic	50	10	21-1800
C67	1n	Chip Ceramic	50	10	21-1800
Diodes					
D1		Dual Schottky HSMS2805			22-1122
D2		Dual Diode BAV99			22-1096
D3		Not used			
D4		Dual Schottky HSMS2805			22-1122

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Transistors					
Q1		BSR18A			22-6199
Q2		BFR92A			22-6220
Q3		BFR92A			22-6220
Q4		BFR92A			22-6220
Q5		BFR92A			22-6220
Q6		BFR92A			22-6220
Q7		BSR18A			22-6199
Q8		BSR18A			22-6199
Q9		BSR17A			22-6197
Q10		BFR92A			22-6220
Q11		BFR92A			22-6220
Q12		BFR92A			22-6220
Q13		BFR92A			22-6220
Q14		BSR18A			22-6199
Integrated Circuits					
IC1		74LS00D			22-4689
IC2		LM358			22-4277
Inductors	H				
L1	10u	Chip		10	23-7332
L2	39n	Chip		10	23-7303
L3	22n	Chip		20	23-7301
L4	39n	Chip		10	23-7303
L5	39n	Chip		10	23-7303
L6	56n	Chip		10	23-7305
L7	39n	Chip		10	23-7303
L8	270n	Chip		10	23-7313
Connectors					
PL6		Socket Right-angle			23-3482
PL39		Socket Right-angle			23-3482

PARTS LIST

L.O. BOARD ASSEMBLY 19-3032

Fig. 16

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Resistors					
	Ohms		W		
R1	470	Chip	0.125	5	20-5765
R2	2.2k	Chip	0.125	5	20-5796
R3	1k	Chip	0.125	5	20-5792
R4	10k	Chip	0.125	5	20-5768
R5	680	Chip	0.125	5	20-5790
R6	560	Chip	0.125	5	20-5789
R7	100k	Chip	0.125	5	20-5813
R8	56	Chip	0.25	5	20-2560
R9	330	Chip	0.125	5	20-5787
R10	180	Chip	0.125	5	20-5784
R11	1k	Chip	0.125	5	20-5792
R12	47	Chip	0.125	5	20-5778
R13	3.9k	Chip	0.125	5	20-5798
R14	2k	Potentiometer			20-7125
R15	8.2k	Chip	0.125	5	20-5767
R16	150	Chip	0.125	5	20-5783
R17	100	Carbon Film	1	5	20-4651
R18	0	Chip	0.125		20-5870
R19	100	Chip	0.125	5	20-5764
R20	2.7k	Chip	0.125	5	20-5766
R21	100	Chip	0.125	5	20-5764
R22	220	Chip	0.125	5	20-5785
R23	470k	Chip	0.125	5	20-5769
R24	10k	Chip	0.125	5	20-5768
R25	56	Chip	0.125	5	20-5779
R26	10k	Chip	0.125	5	20-5768
R27	470	Chip	0.125	5	20-5765
R28	10k	Chip	0.125	5	20-5768
R29	33k	Chip	0.125	5	20-5807
R30	33k	Chip	0.125	5	20-5807
R31	10	Chip	0.125	5	20-5771
R32	68	Chip	0.125	5	20-5780
R33	10k	Chip	0.125	5	20-5768
R34 *	15k	Chip	0.125	5	20-5803
R35	100k	Chip	0.125	5	20-5522

* NOTE:- R34 is not fitted to Model Serial Numbers 1200 onwards.

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Capacitors	F		V		
C1		Not used			
C2		Not used			
C3		Not used			
C4	22p	Chip Ceramic	50	5	21-1791
C5	22p	Chip Ceramic	50	5	21-1791
C6	10n	Chip Ceramic	50	10	21-1801
C7	1n	Chip Ceramic	50	10	21-1800
C8	10n	Chip Ceramic	50	10	21-1801
C9	15p	Chip Ceramic	50	5	21-1789
C10	15u	Chip Electrolytic	10	-10/+50	21-0903
C11	47p	Chip Ceramic	50	5	21-1795
C12	22p	Chip Ceramic	50	5	21-1791
C13	56p	Chip Ceramic	50	5	21-1796
C14	33n	Chip Ceramic	50	10	21-1808
C15	270p	Chip Ceramic	50	5	21-1803
C16	10n	Chip Ceramic	50	10	21-1801
C17	6.8u	Chip Electrolytic	25	-10/+50	21-0907
C18	10p	Chip Ceramic	50	5	21-1787
C19	6.8p	Chip Ceramic	50	+/-0.25p	21-1785
C20	15u	Chip Electrolytic	10	-10/+50	21-0903
C21	100n	Polyester	63	10	21-4565
C22	1n	Chip Ceramic	50	10	21-1800
C23	15u	Chip Electrolytic	10	-10/+50	21-0903
C24	15u	Chip Electrolytic	10	-10/+50	21-0903
C25	10n	Chip Ceramic	50	10	21-1801
C26	1n	Chip Ceramic	50	10	21-1800
C27	10n	Chip Ceramic	50	10	21-1801
C28	33p	Chip Ceramic	50	10	21-1793
C29	15u	Chip Electrolytic	10	-10/+50	21-0903
C30	1n	Chip Ceramic	50	10	21-1800
C31	10n	Chip Ceramic	50	10	21-1801
C32	15u	Chip Electrolytic	10	-10/+50	21-0903
C33	1n	Chip Ceramic	50	10	21-1800
C34	10n	Chip Ceramic	50	10	21-1801
C35	470p	Chip Ceramic	50	5	21-1804

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
C36	1n	Chip Ceramic	50	10	21-1800
C37	15u	Chip Electrolytic	10	-10/+50	21-0903
C38	1n	Chip Ceramic	50	10	21-1800
Diodes					
D1		BZX84C4V7			22-1882
D2		BBY40			22-1108
D3		BBY40			22-1108
D4		Dual Diode BAW56			22-1094
D5		Not used			
D6		Dual Diode BAW56			22-1094
Transistors					
Q1		BSR17A			22-6197
Q2		BFQ19			22-6221
Q3		BFQ19			22-6221
Q4		BSR18A			22-6199
Q5		BLX65E			22-6222
Integrated Circuits					
IC1		SL562C			22-4315
IC2		NJ8821			22-4788
IC3		74HCT373			22-4847
IC4		SP8716			22-4316
Inductors	H				
L1		Not used			
L2	47n	Chip		10	23-7304
L3	1u	Chip		10	23-7320
L4	22n	Chip		20	23-7301
L5	120n	Chip		10	23-7309
L6	1u	Chip		10	23-7320
L7	120n	Chip		10	23-7309
L8	22n	Chip		20	23-7301
L9	22n	Chip		20	23-7301

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Connectors					
PL8		Socket Right-angle			23-3482
PL33		Socket Right-angle			23-3482
P135		Plug Right-angle 20-Way			23-3484

PARTS LIST

OSCILLATOR ASSEMBLY 19-1147

Fig. 24

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Capacitors	F		V		
C1	100n	Ceramic	50	-20/+80	21-1708
Connector					
SK14		Connector, 5-Way			23-5166
Oscillator					
	10 MHz	Crystal Oscillator			23-9134

PARTS LIST

REFERENCE FREQUENCY MULTIPLIER ASSEMBLY 19-1164

Fig. 26

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Resistors	Ohms		W		
R1	220	Chip	0.125	5	20-5785
R2	10k	Chip	0.125	5	20-5768
R3	12k	Chip	0.125	5	20-5802
R4	1.8k	Chip	0.125	5	20-5795
R5	100k	Chip	0.125	5	20-5813
R6	560k	Chip	0.125	5	20-5817
R7	10k	Chip	0.125	5	20-5768
R8	2.2k	Chip	0.125	5	20-5796
R9	2.2k	Chip	0.125	5	20-5796
R10	560	Chip	0.125	5	20-5789
R11	1.8k	Chip	0.125	5	20-5795
R12	330	Chip	0.125	5	20-5787
R13	2.2k	Chip	0.125	5	20-5796
R14	10k	Chip	0.125	5	20-5768
R15	10k	Chip	0.125	5	20-5768
R16	820	Chip	0.125	5	20-5791
R17	56	Chip	0.125	5	20-5779
R18	330	Chip	0.125	5	20-5787
R19	1.8k	Chip	0.125	5	20-5795
R20	56	Chip	0.125	5	20-5779
R21	56	Chip	0.125	5	20-5779
R22	820	Chip	0.125	5	20-5791
R23	1.8k	Chip	0.125	5	20-5795
R24	1.8k	Chip	0.125	5	20-5795
R25	1.8k	Chip	0.125	5	20-5795
R26	1.8k	Chip	0.125	5	20-5795
R27	220	Chip	0.125	5	20-5785
R28	220	Chip	0.125	5	20-5785
R29	220	Chip	0.125	5	20-5785
R30	220	Chip	0.125	5	20-5785
R31	220	Chip	0.125	5	20-5785

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Capacitors					
	F		V		
C1	33n	Chip	50	10	21-1808
C2	2-15p	Variable			21-6043
C3	220p	Chip	50	5	21-1838
C4	220p	Chip	50	5	21-1838
C5	33n	Chip	50	10	21-1808
C6	10n	Chip	50	20	21-1801
C7	10n	Chip	50	20	21-1801
C8	10n	Chip	50	20	21-1801
C9	10n	Chip	50	20	21-1801
C10	10n	Chip	50	20	21-1801
C11	10n	Chip	50	20	21-1801
C12	10n	Chip	50	20	21-1801
C13	33n	Chip	50	10	21-1808
C14	33n	Chip	50	10	21-1808
C15	10n	Chip	50	20	21-1801
Diodes					
D1		Varactor (MV1640)			22-1097
D2		Silicon (BAS16)			22-1093
D3		Voltage Regulator (BZX84C4V7)			22-1882
D4		Silicon (BAV99)			22-1096
D5		Silicon (BAV99)			22-1096
Transistors					
Q1		3904			22-6197
Q2		3906			22-6199
Q3		3906			22-6199
Q4		3904			22-6197
Q5		3904			22-6197
Q6		3904			22-6197
Q7		3904			22-6197
Integrated Circuits					
IC1		Not used			
IC2		741			22-4292
IC3		MC10102			22-4514
IC4		74LS132			22-4582

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Connectors					
SK16		Socket, 5-Way			23-5166
SK17		Socket, 10-Way			23-5167
Transformers					
T1		Transformer to Racal-Dana specification			17-3226

PARTS LIST

REFERENCE FREQUENCY DOUBLER ASSEMBLY 19-1238

Fig. 31

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Resistors	Ohms		W		
R1	33	Chip	0.125	5	20-5776
R2	100	Chip	0.125	5	20-5764
R3	100	Chip	0.125	5	20-5764
R4	1k	Chip	0.125	5	20-5792
R5	470	Chip	0.125	5	20-5765
R6	470	Chip	0.125	5	20-5765
R7	1.5k	Chip	0.125	5	20-5794
R8	3.9k	Chip	0.125	5	20-5798
R9	3.9k	Chip	0.125	5	20-5798
R10	1.5k	Chip	0.125	5	20-5794
R11	1k	Chip	0.125	5	20-5792
R12	39k	Chip	0.125	5	20-5808
R13	15k	Chip	0.125	5	20-5803
R14	330k	Chip	0.125	5	20-5816
R15	10k	Chip	0.125	5	20-5768
R16	1k	Chip	0.125	5	20-5792
R17	3.9k	Chip	0.125	5	20-5798
R18	3.9k	Chip	0.125	5	20-5798
R19	100	Chip	0.125	5	20-5764
R20	1k	Chip	0.125	5	20-5792
Capacitors	F		V		
C1	10n	Chip	50	20	21-1801
C2	10n	Chip	50	20	21-1801
C3	10n	Chip	50	20	21-1801
C4	10n	Chip	50	20	21-1801
C5	10n	Chip	50	20	21-1801
C6	10n	Chip	50	20	21-1801
C7	10n	Chip	50	20	21-1801
C8	10n	Chip	50	20	21-1801

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Diodes					
D1		Silicon (1N4149)			22-1029
D2		Silicon (1N4149)			22-1029
Transistors					
Q1		2N3906			22-6008
Q2		2N3906			22-6008
Q3		2N3904			22-6007
Q4		2N3904			22-6007
Q5		2N3904			22-6007
Q6		2N3904			22-6007
Inductors					
	H				
L1	100u	Choke		10	23-7213
T1		10.7 MHz IF Transformer			23-7149
T2		10.7 MHz IF Transformer			23-7149

PARTS LIST

OSCILLATOR ASSEMBLY 19-1208

Fig. 29

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Capacitors	F		V		
C1	100n	Ceramic	50	20	21-1708
Connectors					
SK14		Connector, 5-Way			23-5166
Oscillator					
	10 MHz	Oscillator, temperature compensated			23-9135

PARTS LIST

SAMPLER/POWER LIMITER BRACKET ASSEMBLY

	Description	Part Number	Qty
Connectors			
	Precision 'N' Adaptor	17-1514	1
Modules			
	Sampler Assembly	17-1102	1
	Power Limiter Assembly (Option 11)	17-1103	1
Miscellaneous			
	Bracket	11-3045	1
	Screw, Pan-head M3 x 5	24-7720	2
	Washer, Plain M3	24-2703	2
	Washer, Crinkle M3	24-2801	2
	Cable Assembly	10-3008	1
	Shrink Sleeving for cable connections	25-5161	20 mm

PARTS LIST

BATTERY PACK ASSEMBLY 11-9009

Fig. 17

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
CHASSIS COMPONENTS					
	Ohms		W		
R1	5.6		10	5	20-5081
		Battery Chassis Assembly (Complete with batteries B1 and B2)			11-1723
		Cableform			10-2906
FS2		Fuselink 1.25 in x 0.25 in 3AT			23-0069
FS3		Fuselink 1.25 in x 0.25 in 3AT			23-0069
BATTERY BOARD ASSEMBLY 19-3049					
Resistors					
	Ohms		W		
R1	39	Carbon Film	0.25	5	20-3470
R2	1M	Chip	0.125	5	20-5770
R3	4.7k	Chip	0.125	5	20-5799
R4	1M	Chip	0.125	5	20-5770
R5	56	Carbon Film	0.25	5	20-2560
R6	10M	Carbon Film	0.25	10	20-2106
R7	1M	Chip	0.125	5	20-5770
R8	560k	Chip	0.125	5	20-5817
R9	560k	Chip	0.125	5	20-5817
R10	50k	Potentiometer			20-7086
R11	56k	Chip	0.125	5	20-5810
R12	1k	Chip	0.125	5	20-5792
R13	22k	Chip	0.125	5	20-5805
R14	1M	Chip	0.125	5	20-5770
R15	560k	Chip	0.125	5	20-5817

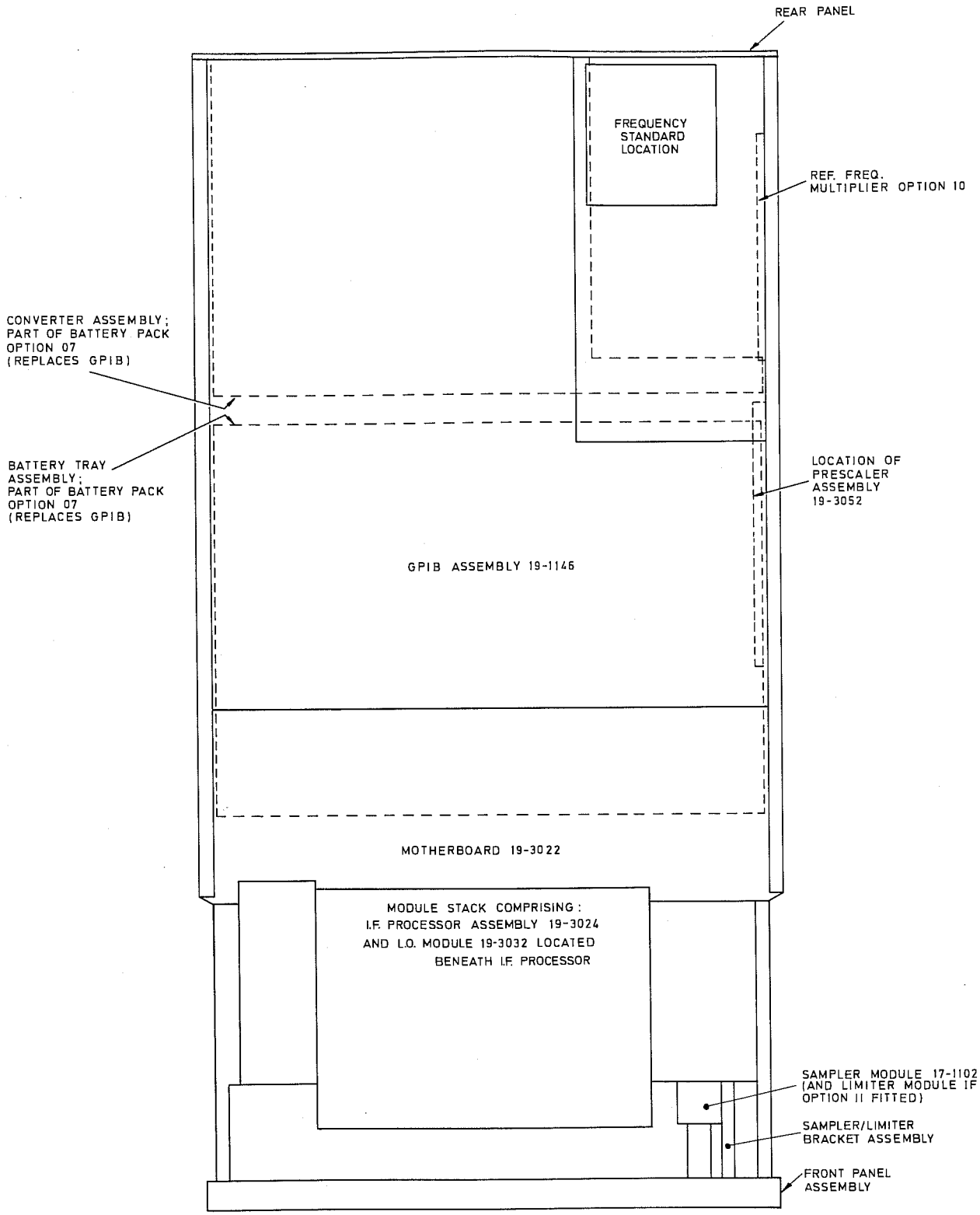
Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
R16	1M	Chip	0.125	5	20-5770
R17	10k	Chip	0.125	5	20-5768
R18	1M	Chip	0.125	5	20-5770
R19	1M	Chip	0.125	5	20-5770
R20	1M	Chip	0.125	5	20-5770
R21	10M	Carbon Film	0.25	10	20-2106
R22	10k	Chip	0.125	5	20-5768
R23	10k	Chip	0.125	5	20-5768
R24	100k	Chip	0.125	5	20-5813
R25	56k	Chip	0.125	5	20-5810
R26	220	Chip	0.125	5	20-5785
R27	1k	Carbon Film	0.25	5	20-2102
R28	20k	Potentiometer			20-7116
R29	22k	Chip	0.125	5	20-5805
R30	22k	Chip	0.125	5	20-5805
R31	4.7k	Chip	0.125	5	20-5799
R32	4.7k	Chip	0.125	5	20-5799
R33	180	Carbon Film	0.25	5	20-2181
R34	68	Carbon Film	0.25	5	20-3680
R35	1M	Chip	0.125	5	20-5784
R36	50k	Potentiometer			20-7086
R37	220k	Chip	0.125	5	20-5829
R38	10k	Chip	0.125	5	20-5768
R39	3.9k	Chip	0.125	5	20-5798
R40	560	Chip	0.125	5	20-5789
R41	39k	Chip	0.125	5	20-5808
R42	1k	Chip	0.125	5	20-5792
R43	27k	Chip	0.125	5	20-5806
R44	10k	Chip	0.125	5	20-5768
R45	8.2k	Chip	0.125	5	20-5767
R46	1k	Chip	0.125	5	20-5792
R47	1M	Chip	0.125	5	20-5770
R48	100k	Chip	0.125	5	20-5813
R49	10M	Carbon Film	0.25	10	20-2106
R50	150	Carbon Film	0.5	5	20-3151
R51	10k	Chip	0.125	5	20-5768
R52	47k	Chip	0.125	5	20-5809

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Capacitors					
	F		V		
C1	330n	Electrolytic	50		21-0793
C2	10u	Electrolytic	16		21-0775
C3	100n	Ceramic			21-1708
C4	100n	Ceramic			21-1708
C5	220p	Chip			21-1838
C6	330n	Electrolytic	50		21-0793
C7	10n	Chip			21-1801
C8	1.5u	Electrolytic	50		21-0789
C9	33n	Ceramic			21-1547
C10	22u	Electrolytic	16		21-0776
C11	33u	Electrolytic	25		21-0782
C12	100n	Electrolytic	50		21-0778
C13	10n	Ceramic			21-1752
C14	100n	Electrolytic	50		21-0778
C15	330u	Electrolytic	40		21-0687
C16	100n	Ceramic			21-1708
C17		Not used			
C18	10u	Electrolytic	16		21-0716
C19	10u	Electrolytic	16		21-0716
C20	10n	Chip			21-1801
C21	10n	Chip			21-1801
C22	10n	Chip			21-1801
C23	47u	Electrolytic	16		21-0788
C24	47u	Electrolytic	16		21-0788
C25	1u	Electrolytic	50		21-0779
Diodes					
D1		Silicon 1N4002			22-1602
D2		Silicon 1N4149			22-1029
D3		Silicon 1N4149			22-1029
D4		Silicon 1N4149			22-1029
D5		Silicon 1N4149			22-1029

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
D6		Silicon 1N4149			22-1029
D7		Avalanche BYV95A			22-2009
D8		Not used			
D9		Schottky MBR340P			22-2008
D10		Schottky MBR340P			22-2008
D11		Voltage Regulator BZX79B3V9			22-1825
D12		Silicon 1N4002			22-1602
D13		Voltage Regulator BZX79B5V6			22-1856
D14		Silicon BA516			22-1093
D15		Silicon 1N5401			22-2010
D16		Silicon 1N4149			22-1029
Transistors					
Q1		2N3904			22-6007
Q2		2N3906			22-6008
Q3		2N3904			22-6007
Q4		2N3906			22-6008
Q5		BUZ21			22-6208
Q6		2N3904			22-6007
Q7		MJE371			22-6139
Q8		2N3904			22-6007
Q9		2N3904			22-6007
Q10		BDT92			22-6208
Integrated Circuits					
IC1		4072			22-4770
IC2		4030			22-4729
IC3		4001			22-4738
IC4		CA358E			22-4295
IC5		4001			22-4738
IC6		LM339N			22-4249
IC7		LAS6320P			22-4291
IC8		78L05			22-4247

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Transformers					
T1					17-4501
Connectors					
SK21		Connector 24-way			23-5169
Miscellaneous					
RLA		Relay			23-7531
SWITCH BOARD ASSEMBLY 19-1242					
Resistors	Ohms		W		
R101	100k	Chip	0.125	5	20-5813
R102	10k	Chip	0.125	5	20-5768
R103	10k	Chip	0.125	5	20-5768
R104	100k	Chip	0.125	5	20-5813
R105	1k	Chip	0.125	5	20-5792
R106	1k	Chip	0.125	5	20-5792
R107	10k	Chip	0.125	5	20-5768
R108	100k	Chip	0.125	5	20-5813
R109	10k	Chip	0.125	5	20-5768
R110	10k	Chip	0.125	5	20-5768
Capacitors	F		V		
C101	220u	Electrolytic	40		21-0768
C102	100n	Ceramic			21-1708
Diodes					
D101		Silicon 1N4002			22-1602
D102		Schottky MBR340P			22-2008

Cct. Ref.	Value	Description	Rating	Tol. %	Part Number
Transistors					
Q101		2N3904			22-6007
Q102		2N3906			22-6008
Q103		2N3906			22-6008
Q104		2N3906			22-6008
Q105		2N3906			22-6008
Miscellaneous					
JK1		Socket			23-3433
S1		Switch SPDT			23-4126
S2		Switch DPDT			23-4127
FS1		Fuselink 1.25 in x 0.25 in 3AT			23-0069
		Fuseholder for FS1			23-0062
		Top for 23-0062			23-0063



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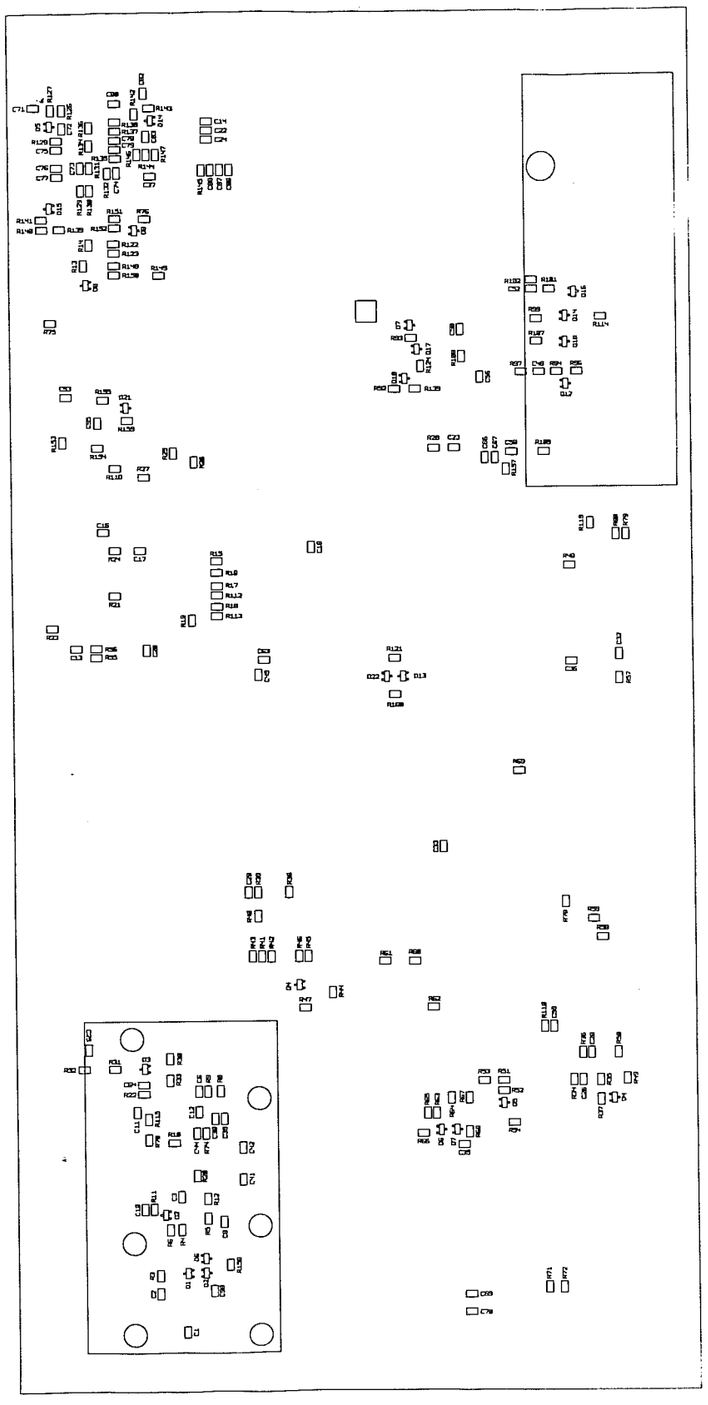
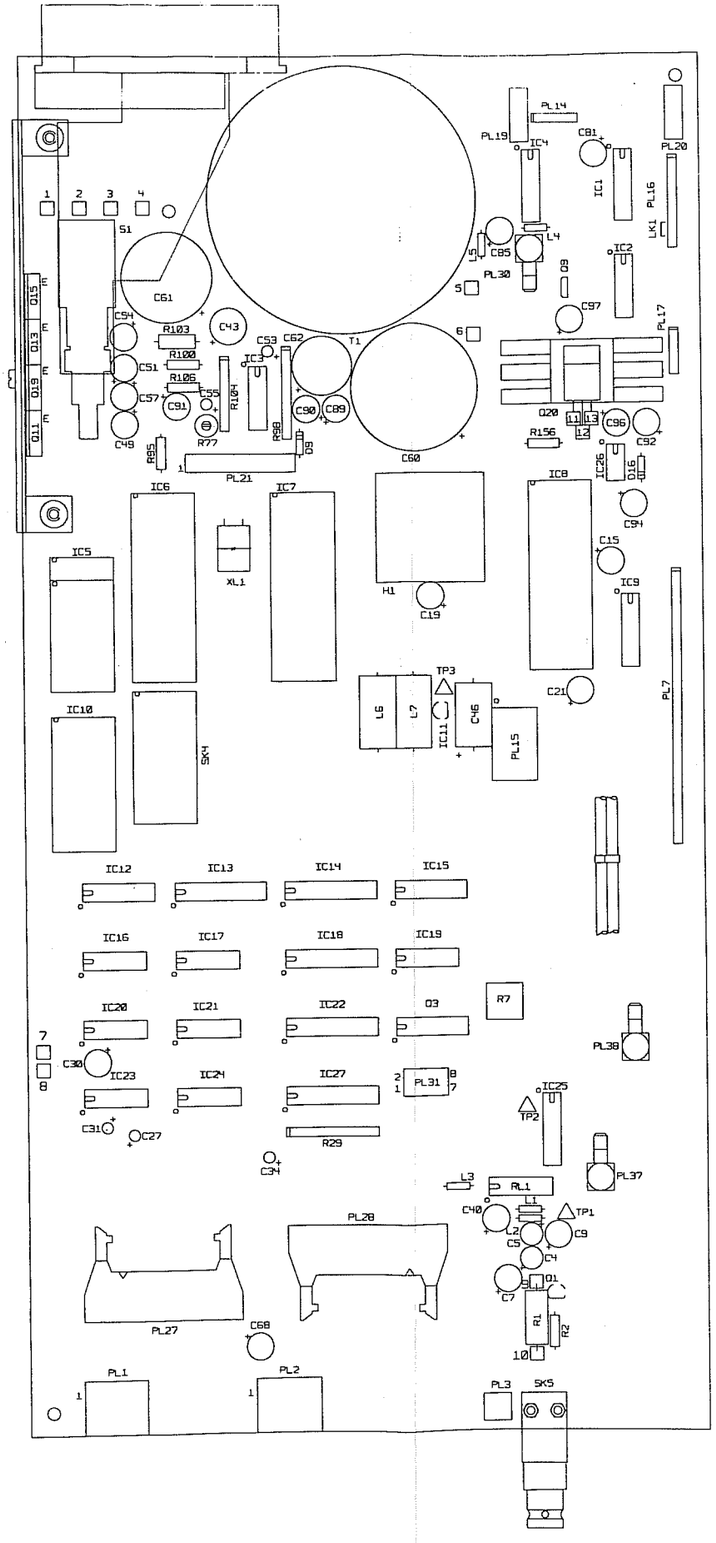
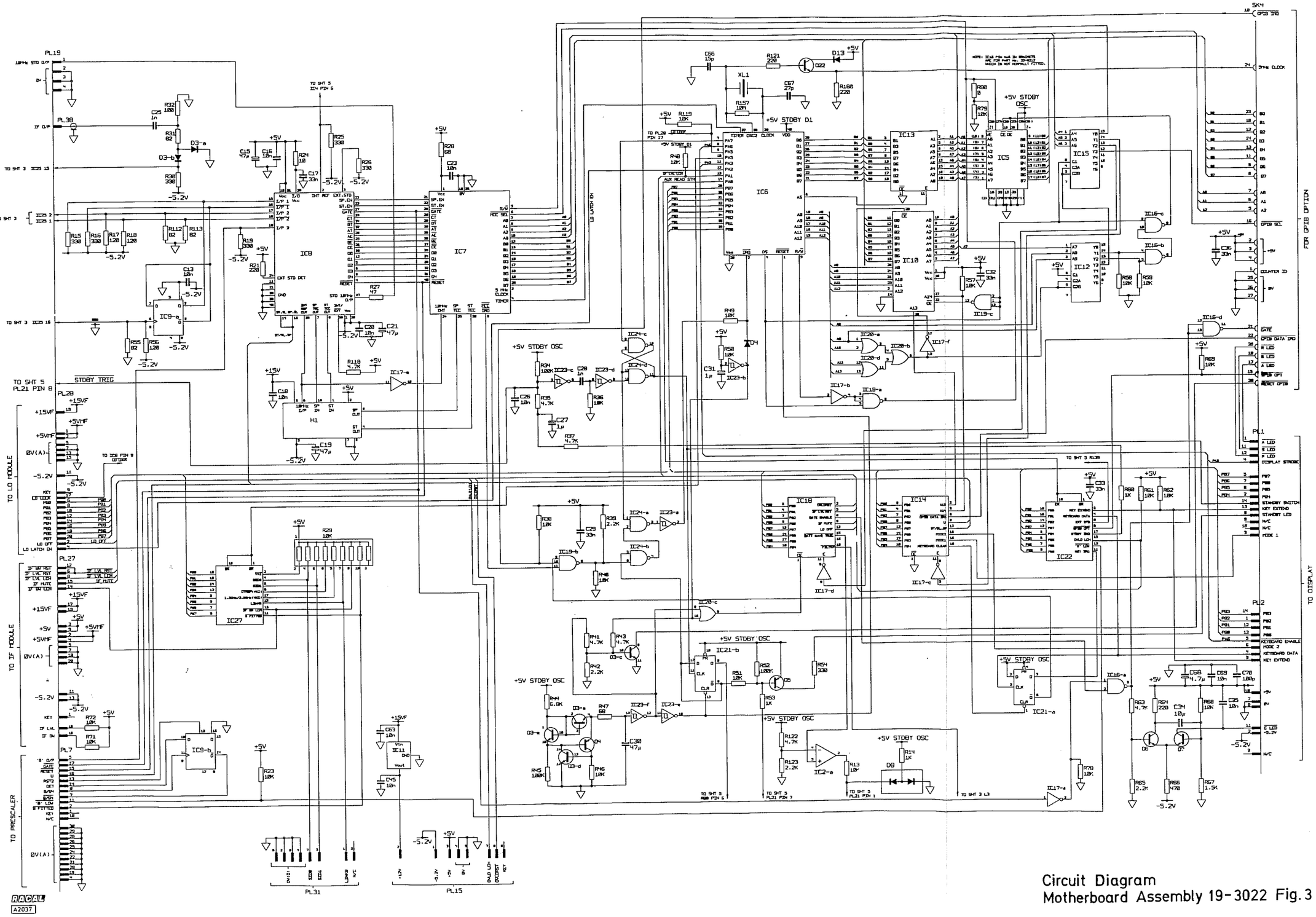
Layout: 2101 Fig. 1

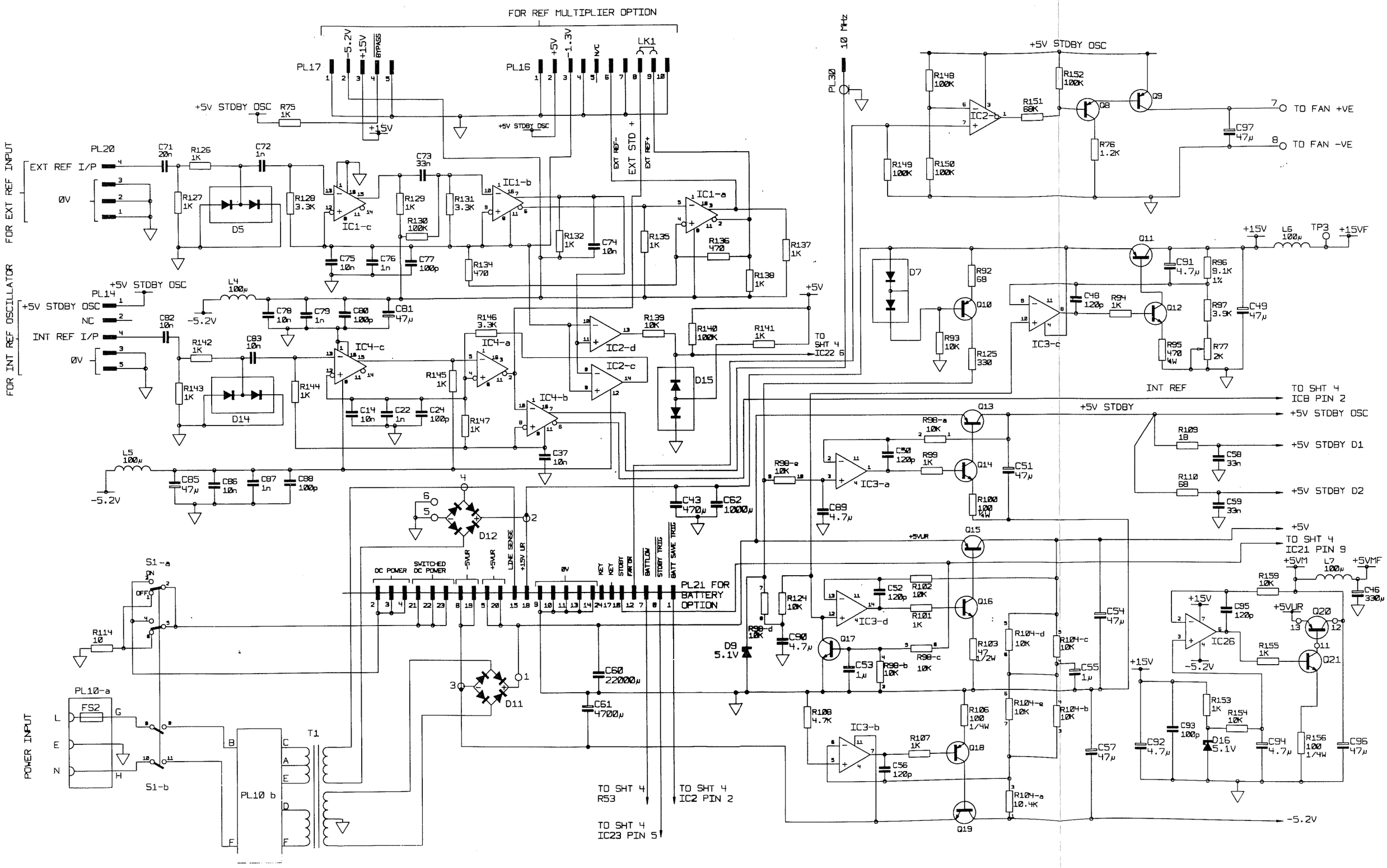




Component Layout
Motherboard Assembly 19-3022 Fig. 2



Circuit Diagram
Motherboard Assembly 19-3022 Fig.3



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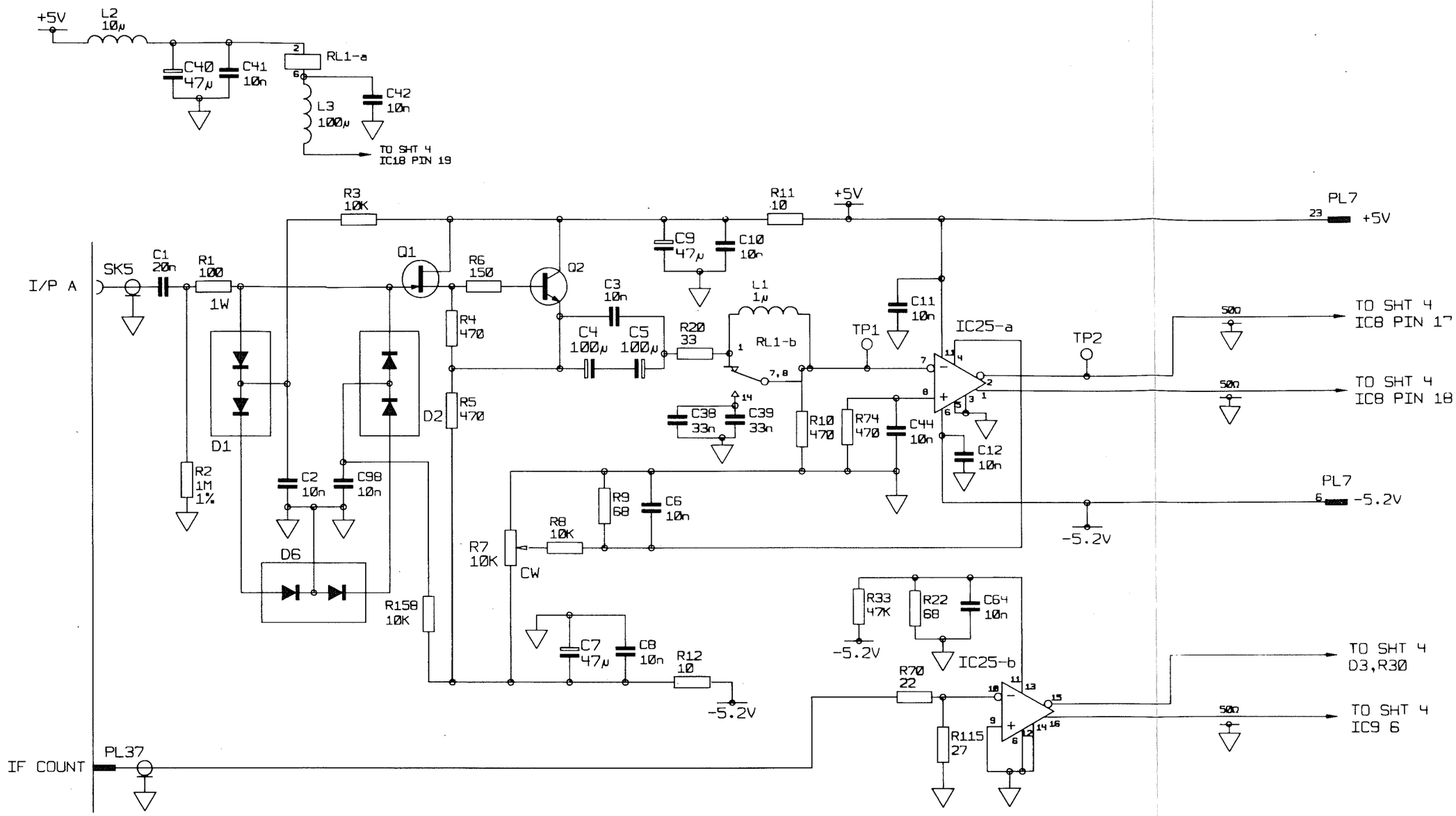
Circuit Diagram
Motherboard Assembly 19-3022 Fig. 4



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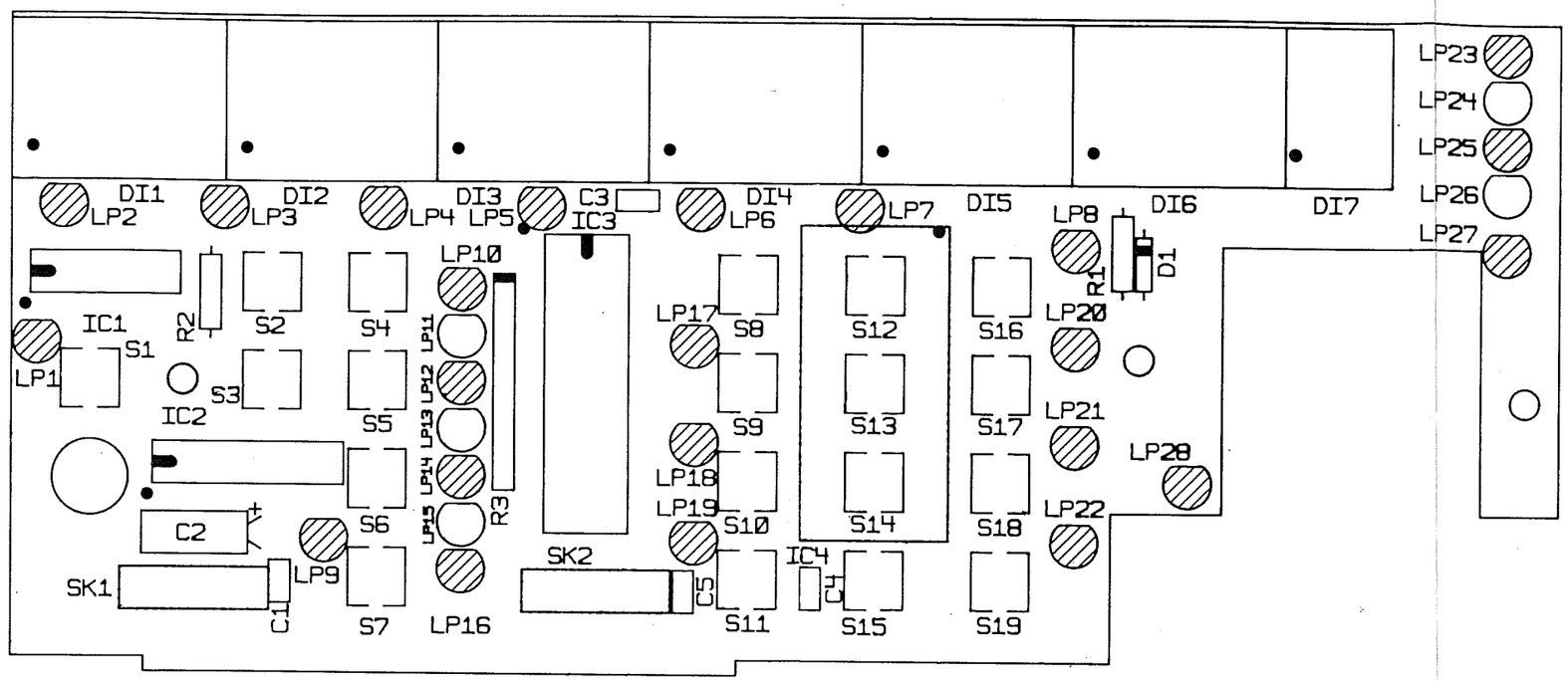
Circuit Diagram
Motherboard Assembly 19-3022 Fig. 5



NOTE: ▨ SHOWS INDICATORS FITTED WITH LIGHT-BLOCK SLEEVING

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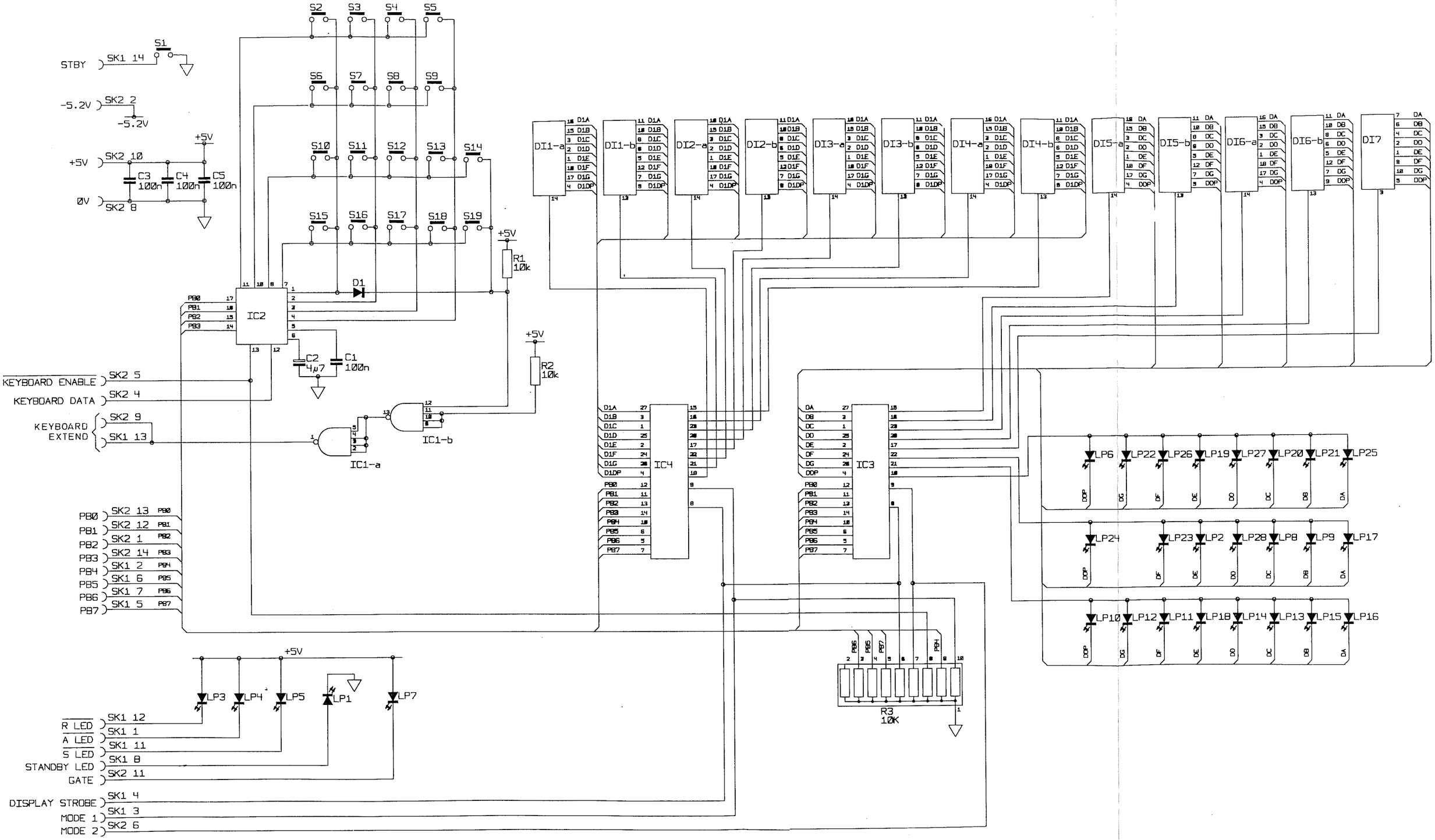
Layout Diagram
Display Assembly 19-3019 Fig. 6



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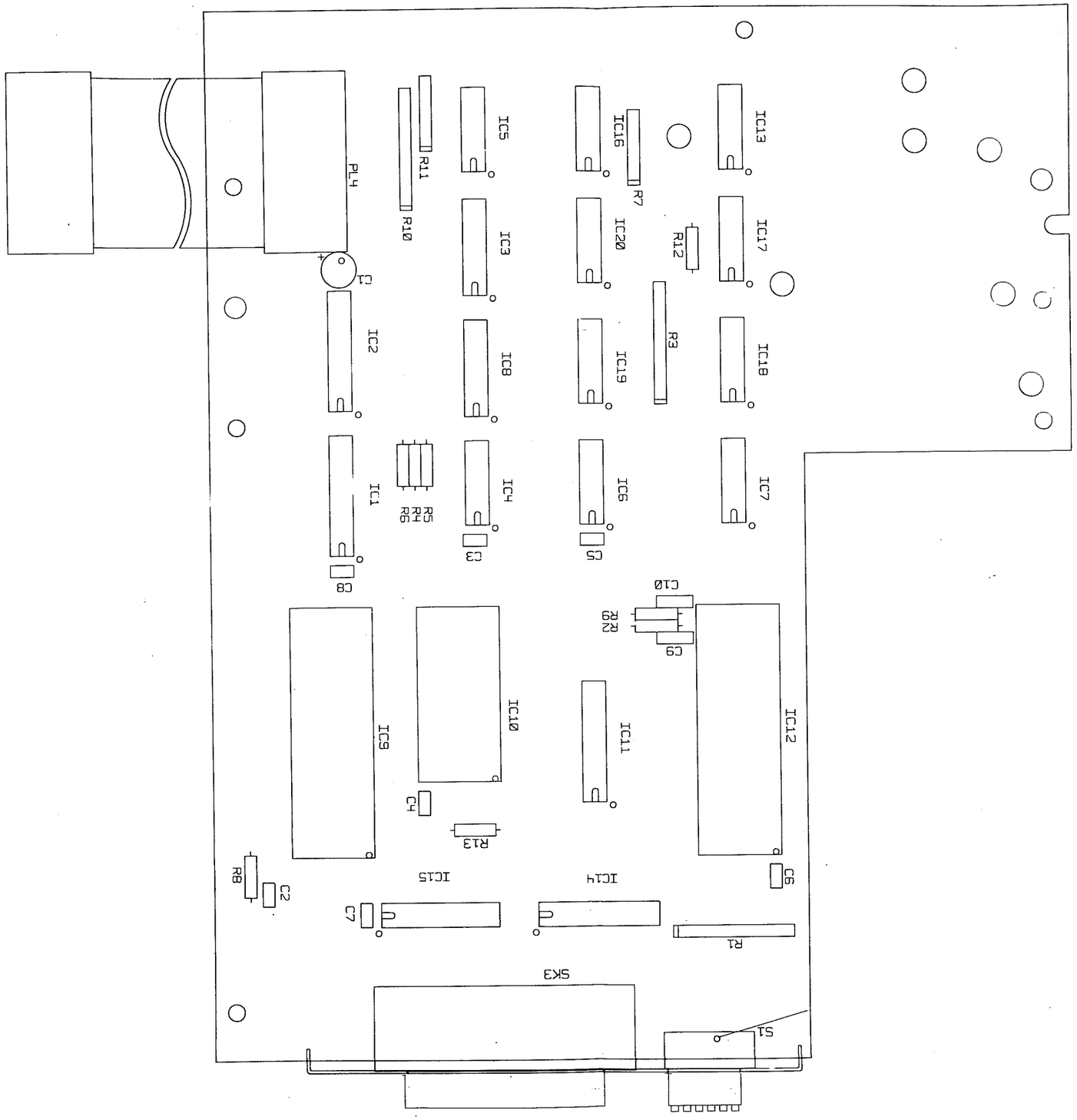
Circuit Diagram
Display Assembly 19-3019 Fig. 7



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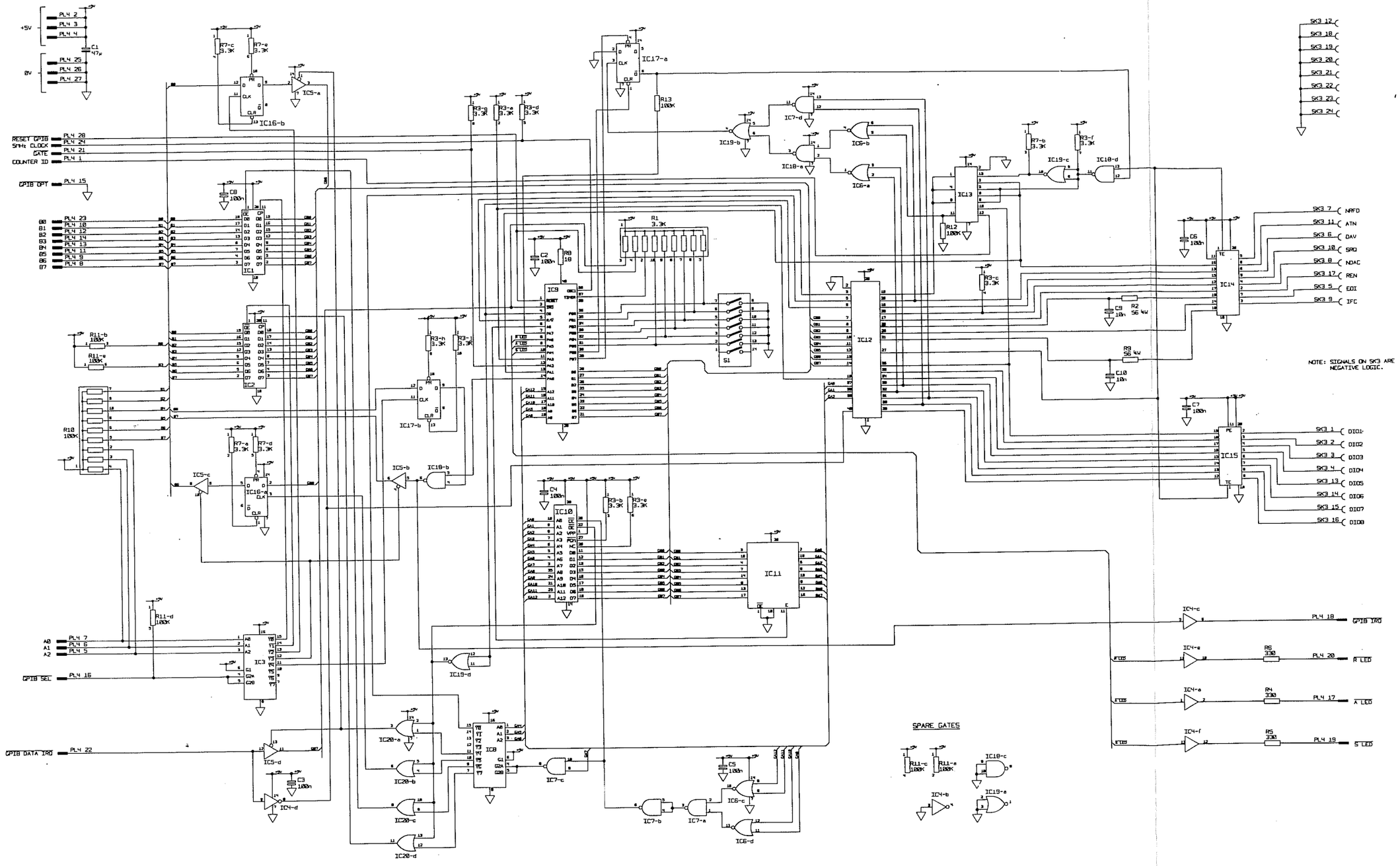
Component Layout:
GPIB Assembly 19-1146 Fig. 8



Circuit Diagram:
GPIB Assembly 19-1146 Fig. 9

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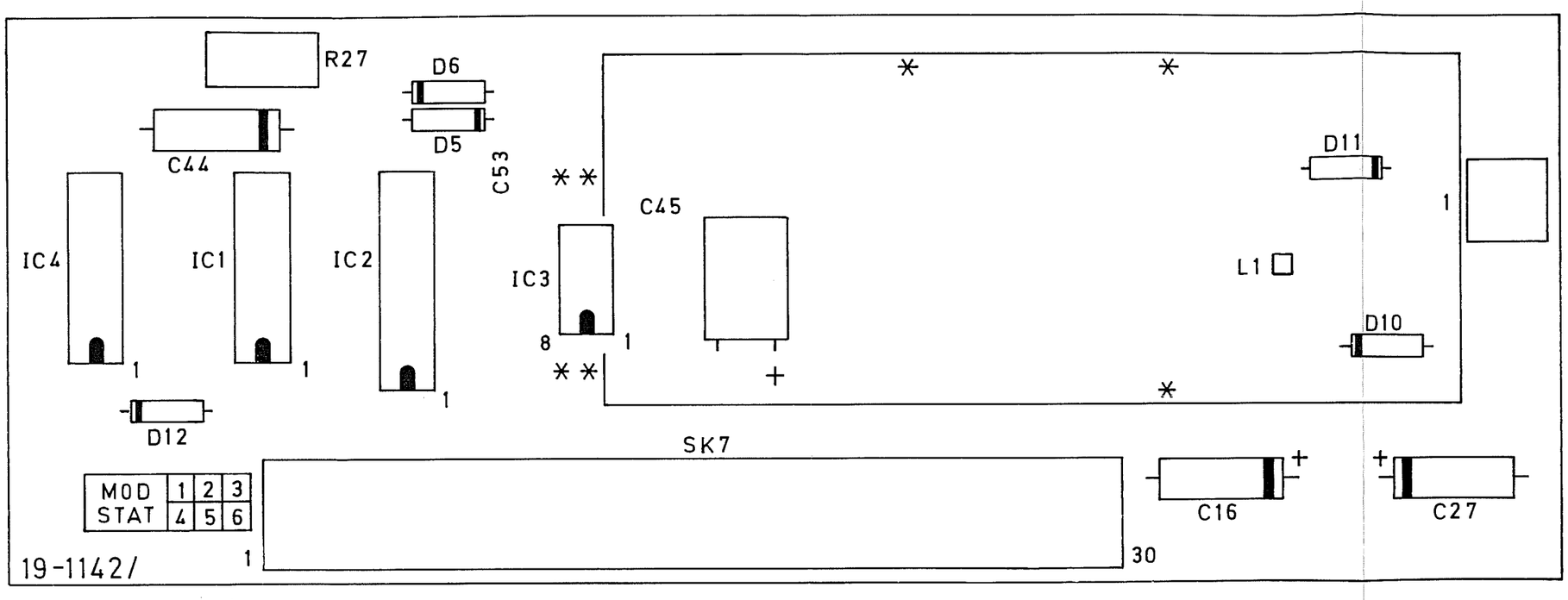

COMPSIDE VIEW

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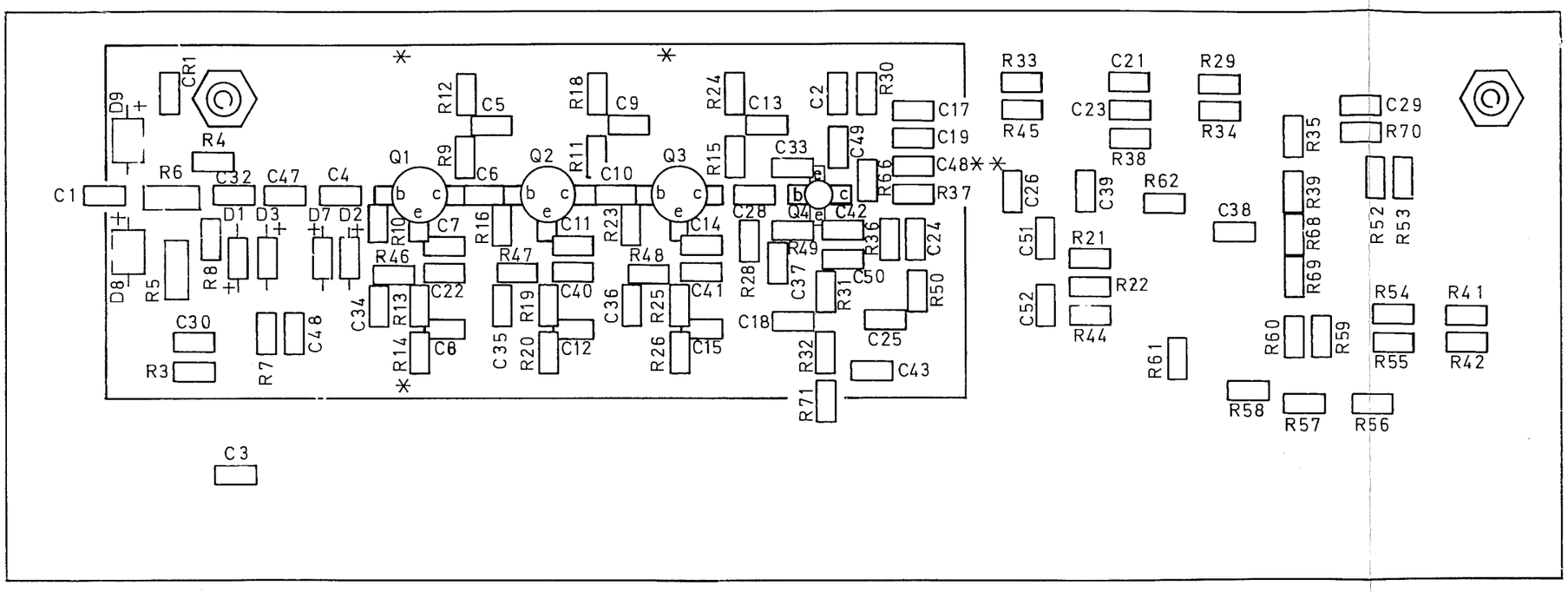
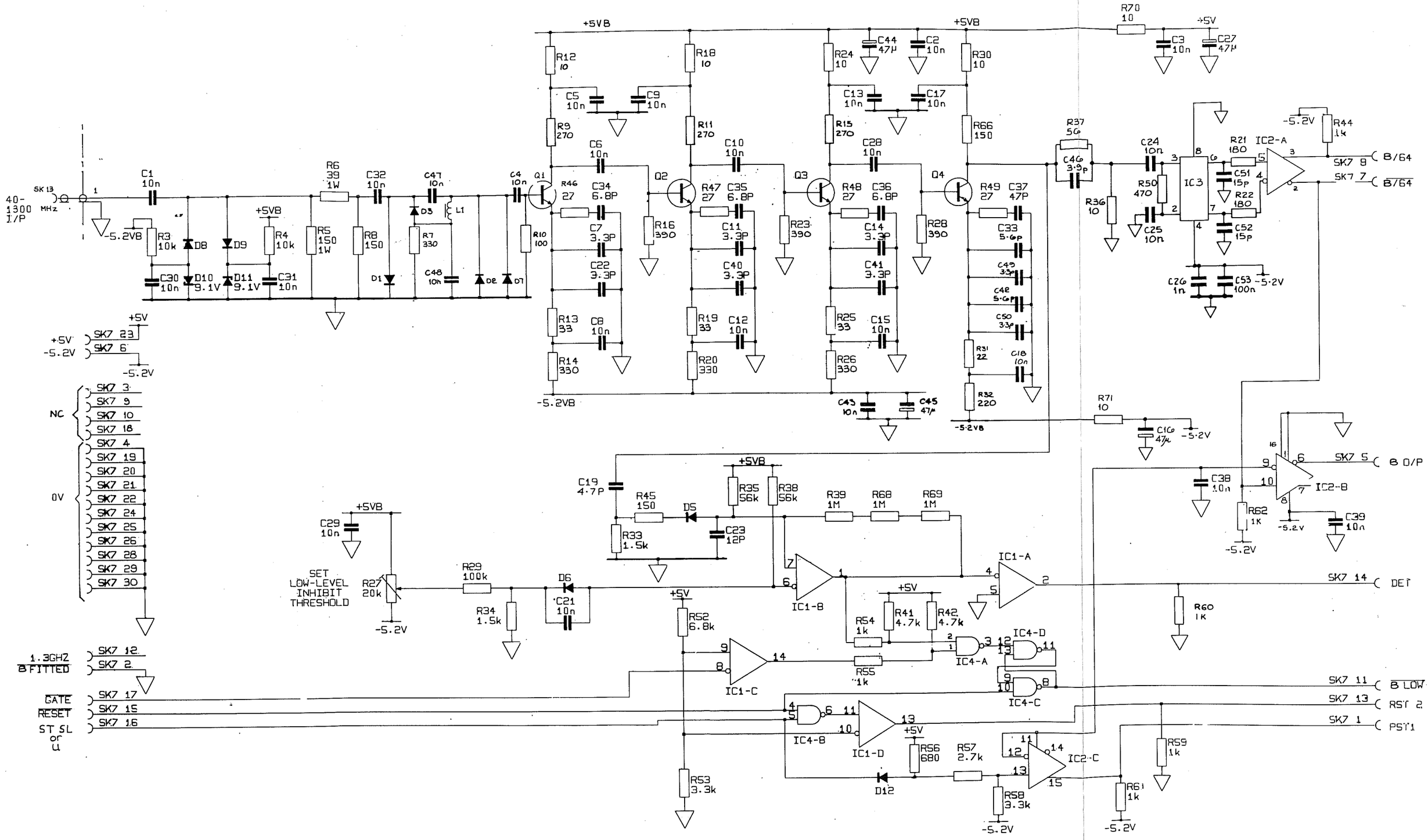
Layout Diagram - Part 1
Prescaler Assembly 19-3052 Fig.10



TRACKSIDE VIEW

A2037

Layout Diagram - Part 2
Prescaler Assembly 19-3052 Fig. 11



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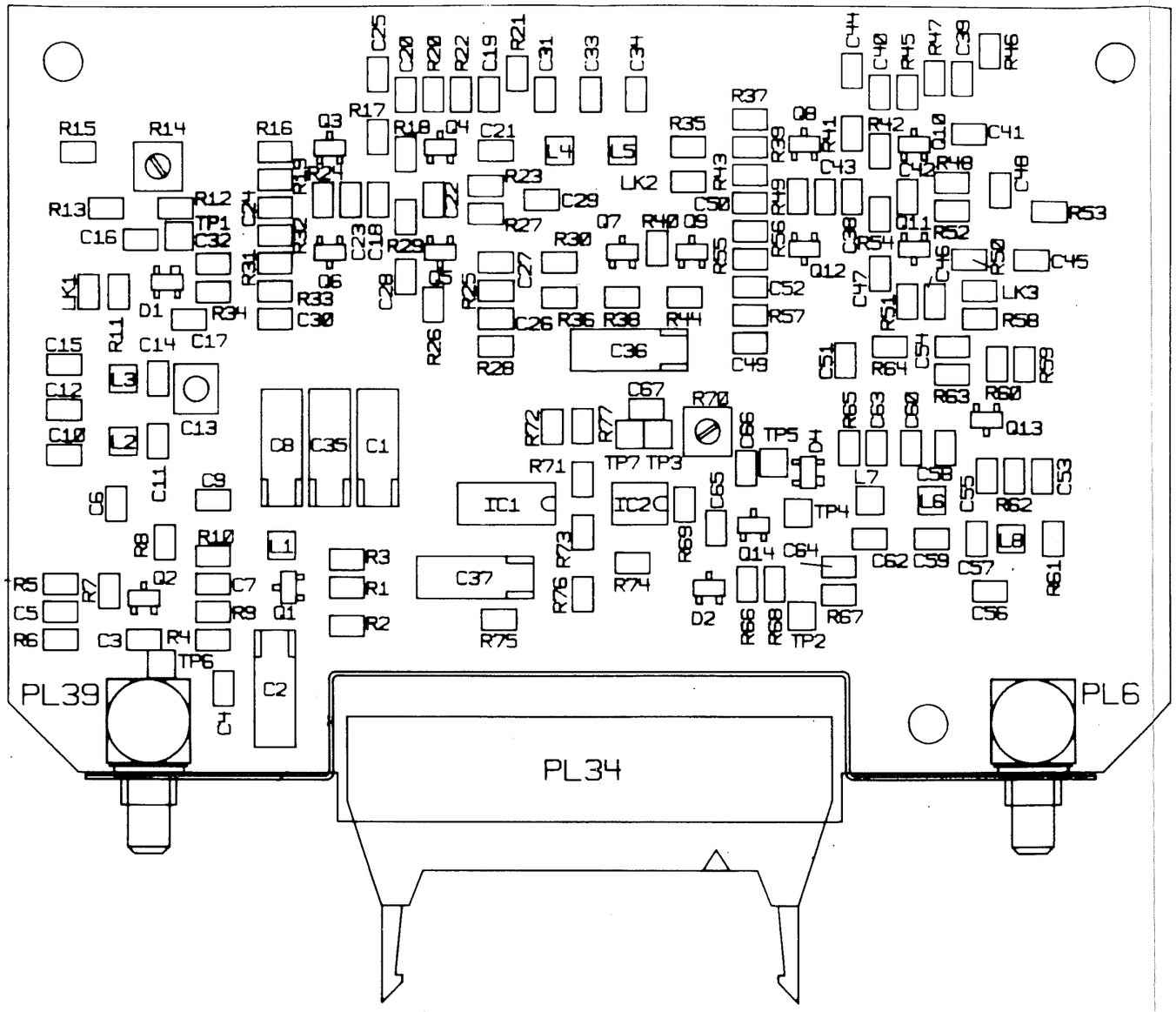
Circuit Diagram
Prescaler Assembly 19-3052 Fig. 12



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Layout Diagram
I. F. Processor Assembly 19-3024 Fig. 13

SAMPLER CURRENT SOURCE

SAMPLER IF AND BIAS FEED

GAIN STAGE

IF BANDWIDTH SET

175MHz LOW PASS FILTER

BANDWIDTH DETECTOR

SYSTEM GAIN SET

DIFFERENTIAL GAIN STAGE

200MHz LOW-PASS FILTER

CURRENT SWITCH

DIFFERENTIAL GAIN STAGE

TEMPERATURE COMPENSATION

BUFFER STAGE

31MHz-122MHz BANDPASS FILTER

LEVEL DETECTOR

THRESHOLD SET

IF BANDWIDTH + LEVEL LATCHES

PL34 15 IF MUTE

PL6 IF COUNT

PL34 16 IF BW

PL34 14 IF BW LCH

PL34 12 IF BW RST

PL34 10 IF LVL

PL34 8 IF LVL LCH

PL34 6 IF LVL RST

N/C PL34 1 POLARIZING KEY

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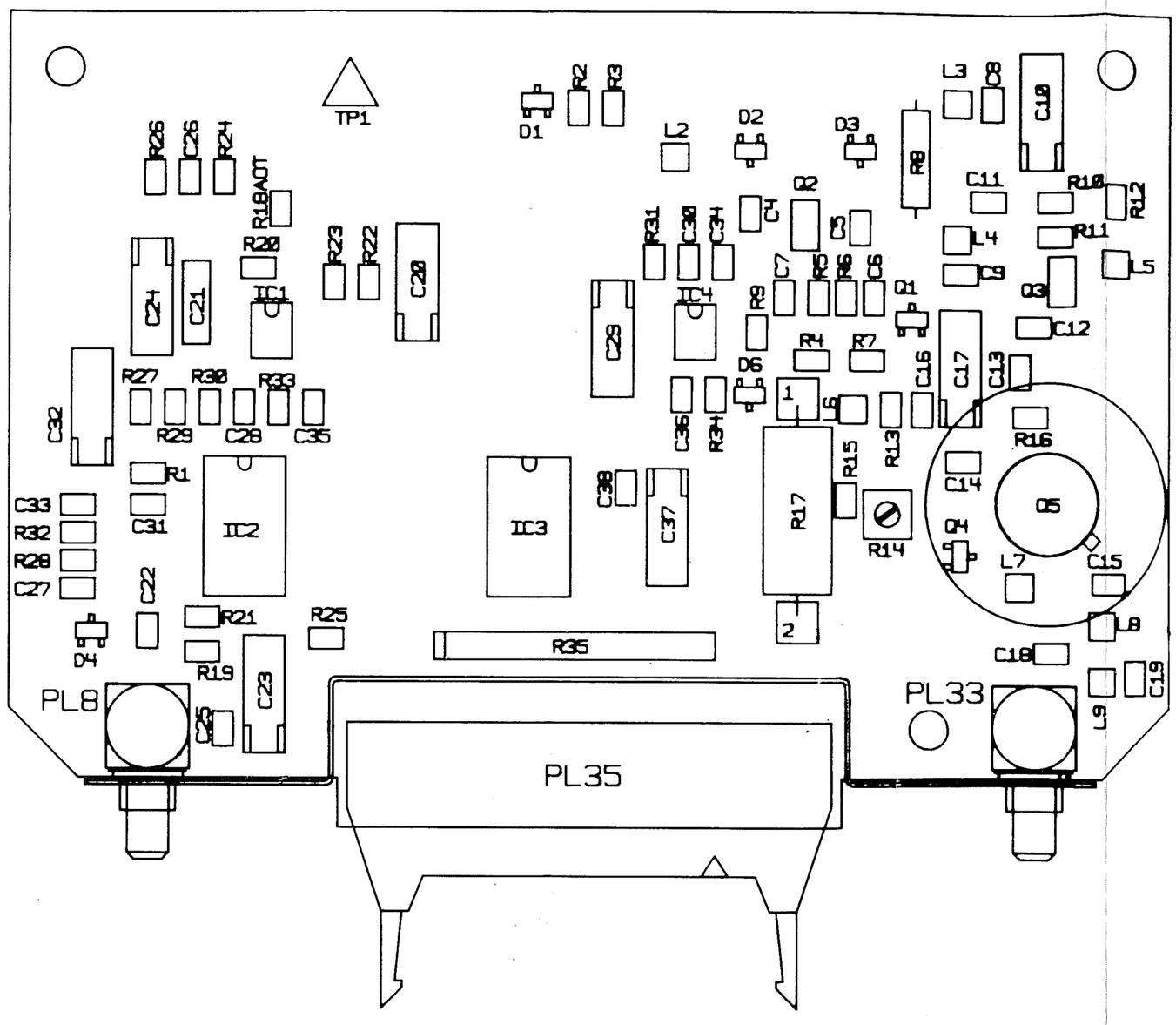
Circuit Diagram
I.F. Processor Assembly 19-3024 Fig. 14



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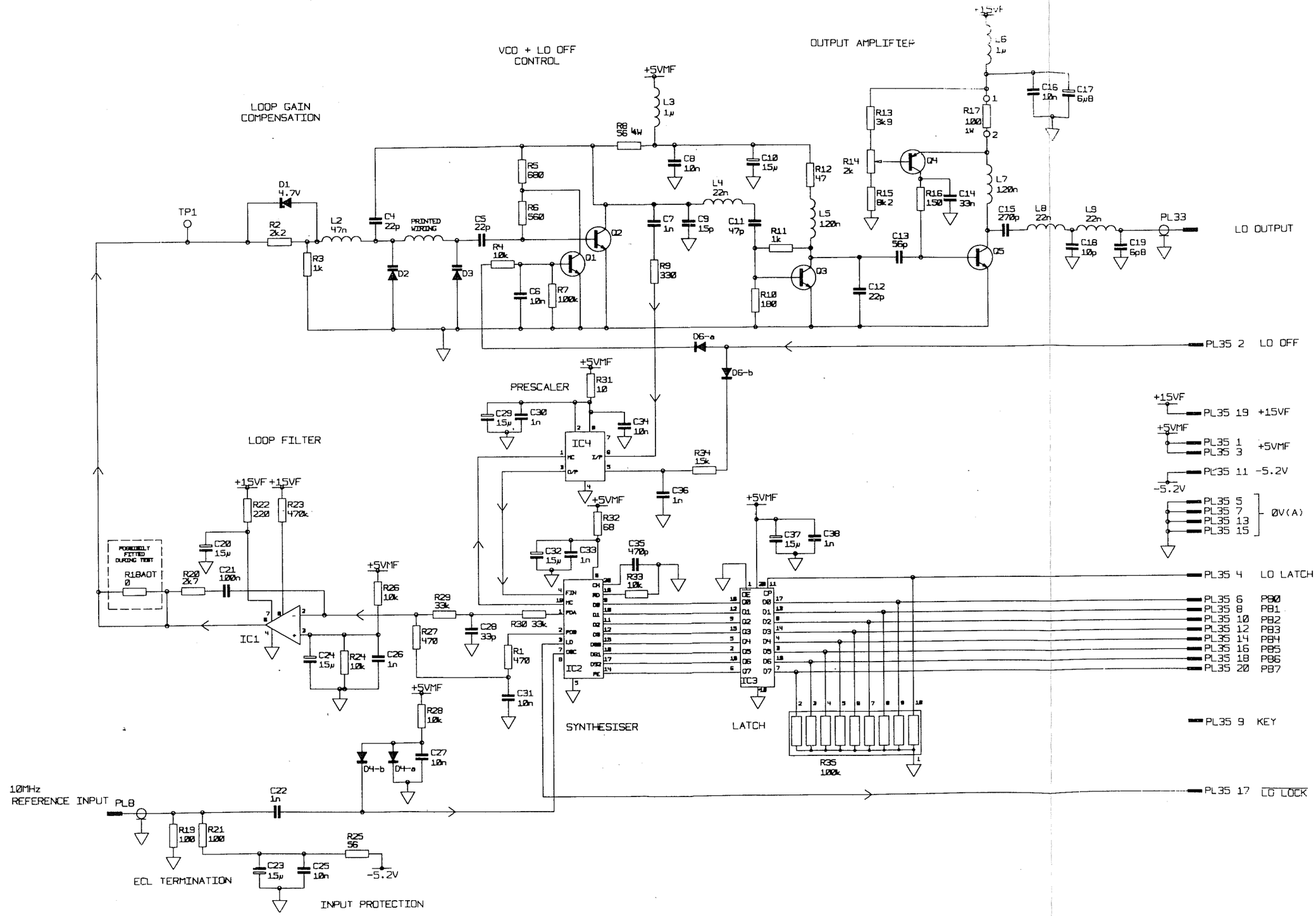
Layout Diagram
Local Oscillator Assembly 19-3032 Fig. 15



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Circuit Diagram
Local Oscillator Assembly 19-3032 Fig. 16

19-3049
BATTERY BD ASSY.

SWITCHED D.C. POWER

KEY

MANAGEMENT CIRCUITS

POWER-DOWN LATCH
PART 19-1242 SWITCH BD. ASSY.

CONVERTER

CHARGER

PART 19-1242
SWITCH BD. ASSY.

11-1723

mOUNTED ON 11-7851

NOT FITTED

STBYTRIG

+15VUR

KEY

+5VUR

0V

-5.2VUR

FAN ON

BATT LOW

RACAL
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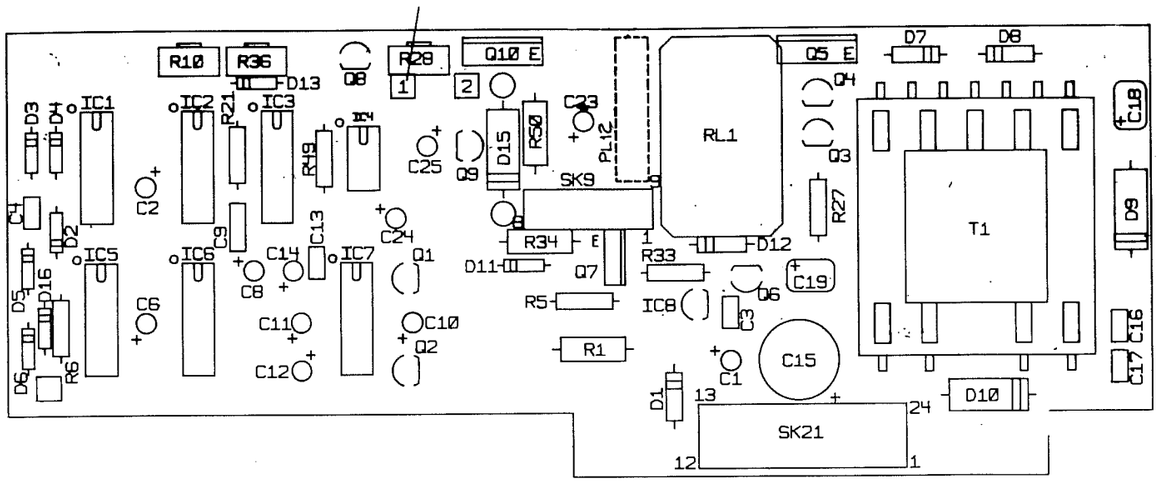
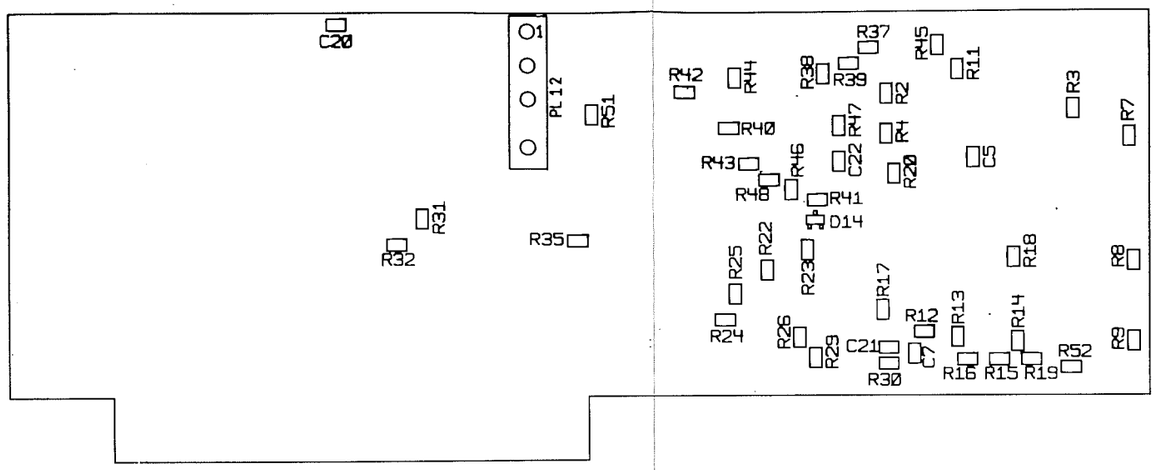
Circuit Diagram
Battery Pack Assembly 11-9009 Fig.17

COMPONENT SIDE VIEW



TRACKSIDE VIEW



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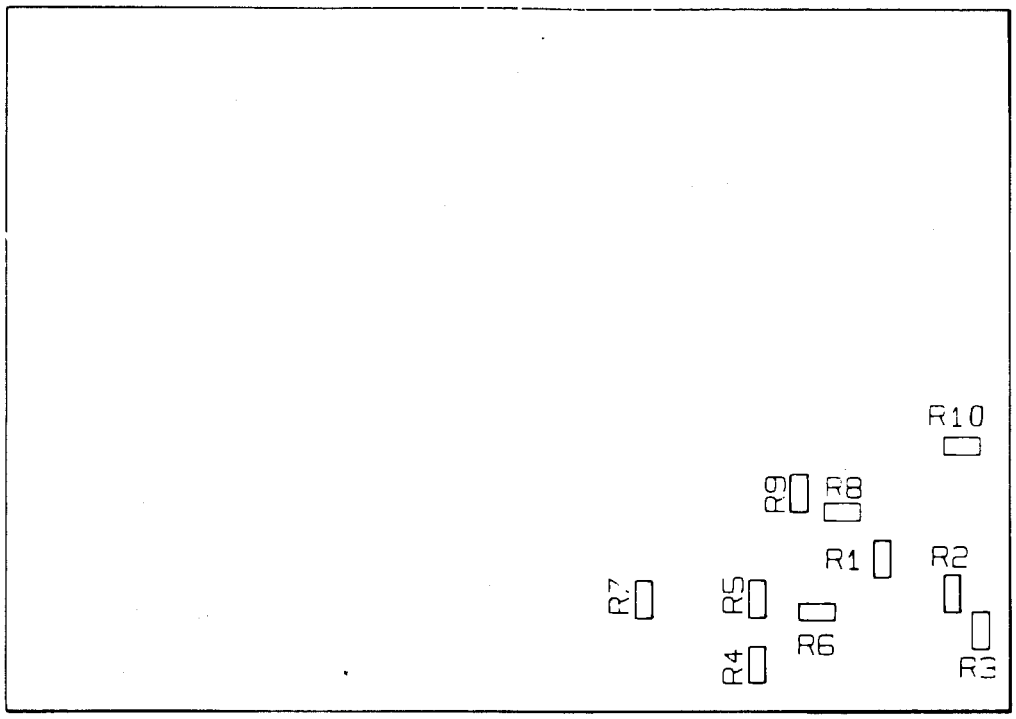
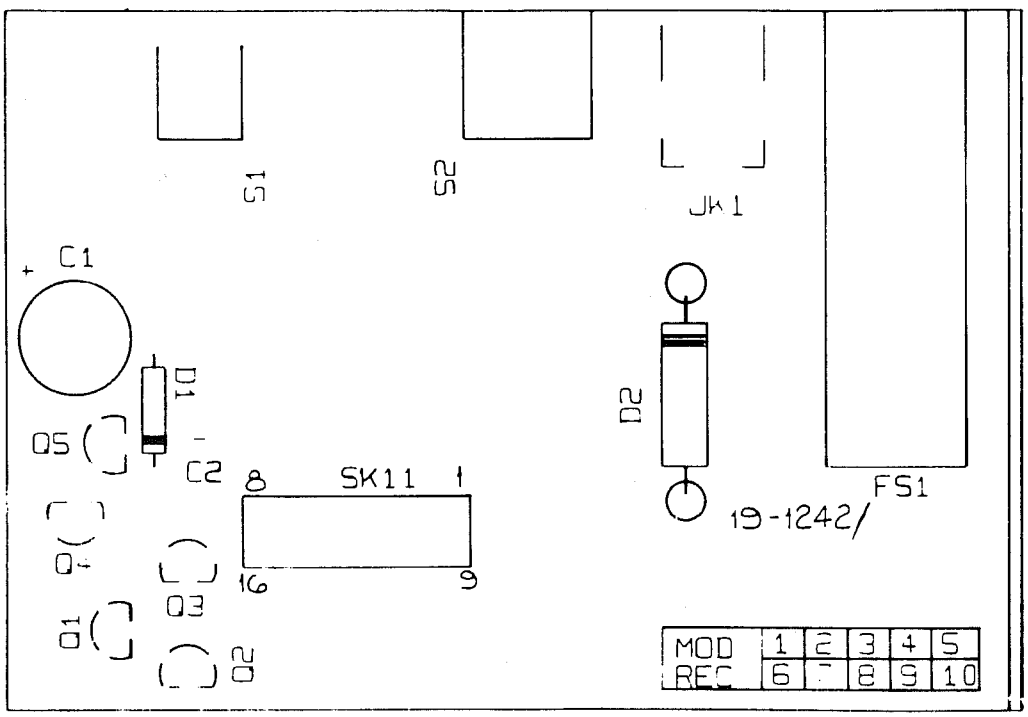
1

Component Layout:
Battery Board Assembly 19-3049 Fig. 18



TRACKSIDE VIEW



COMPONENT SIDE VIEW

Component Layout :
Switch Board Assembly 19-1242

Fig. 19

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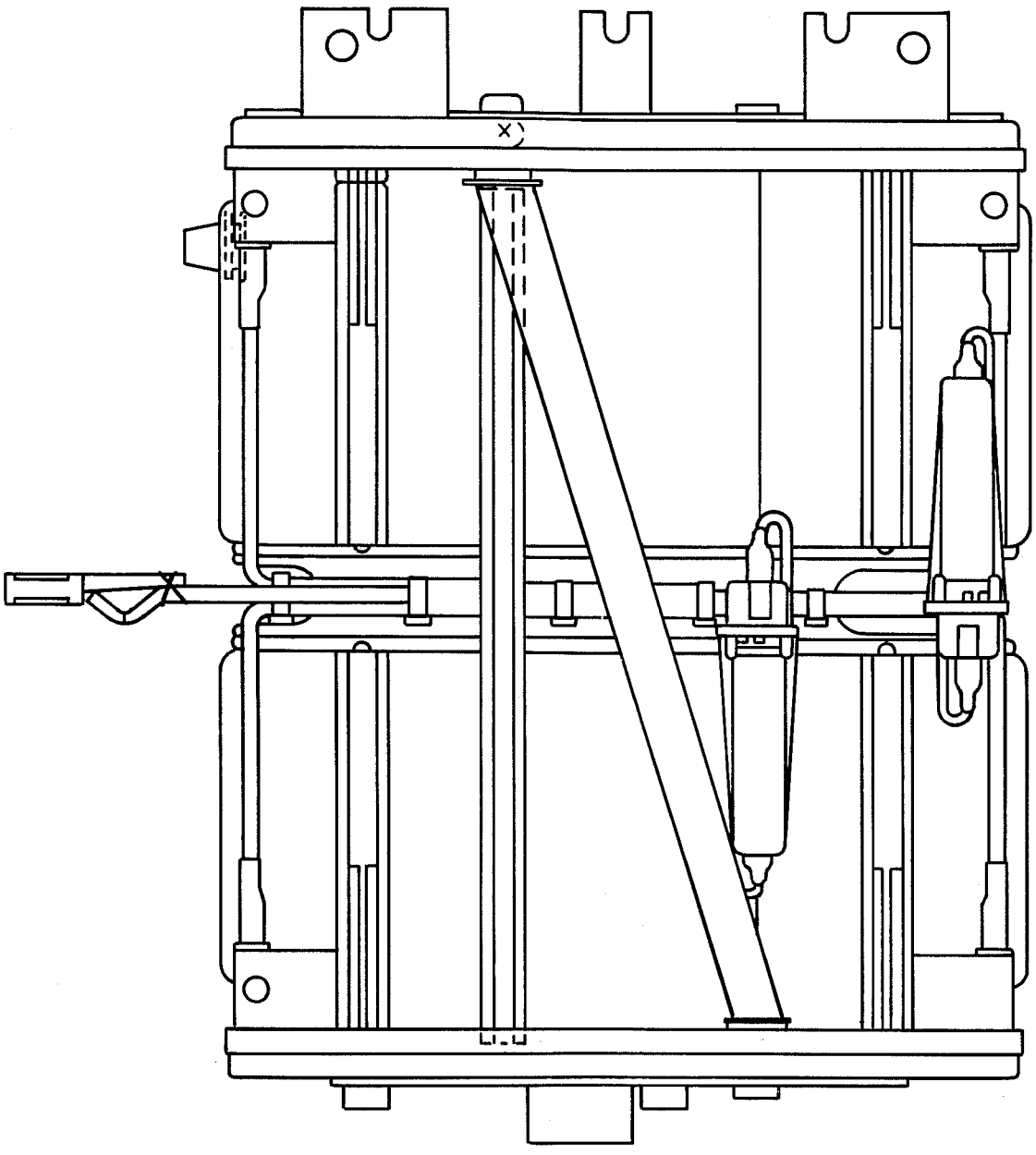

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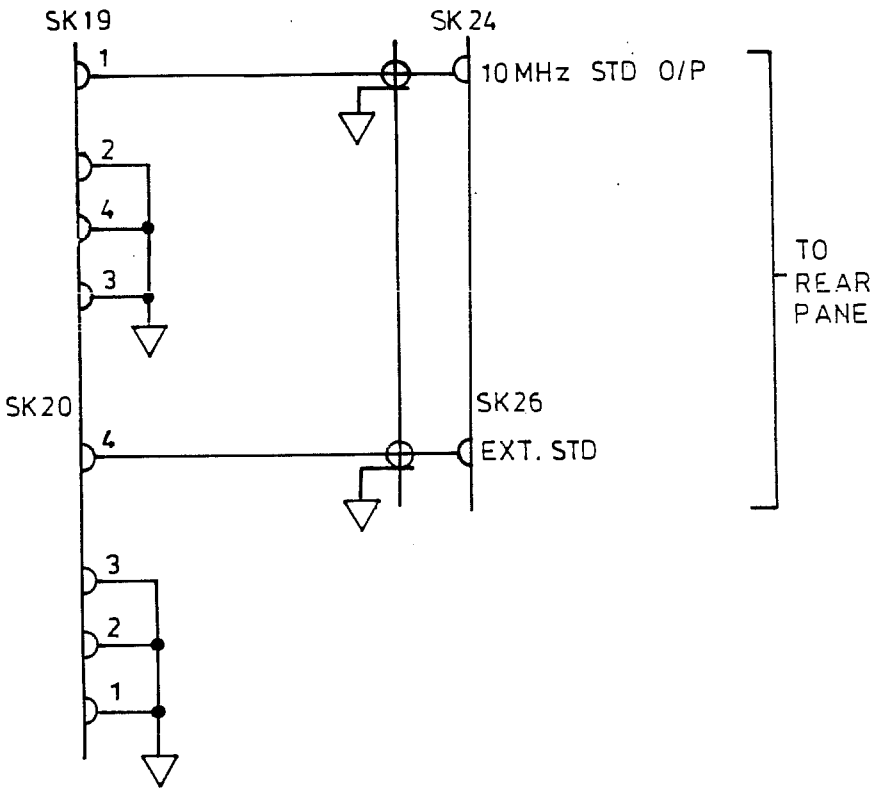
Layout :
Battery Assembly 11-1723 Fig. 20



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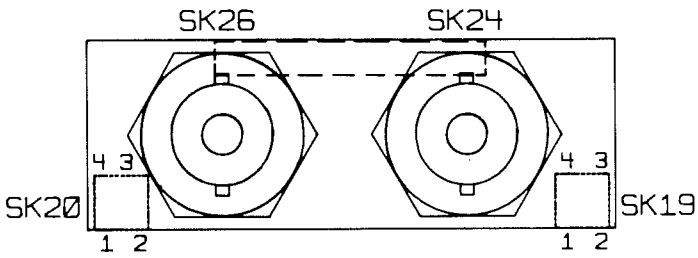
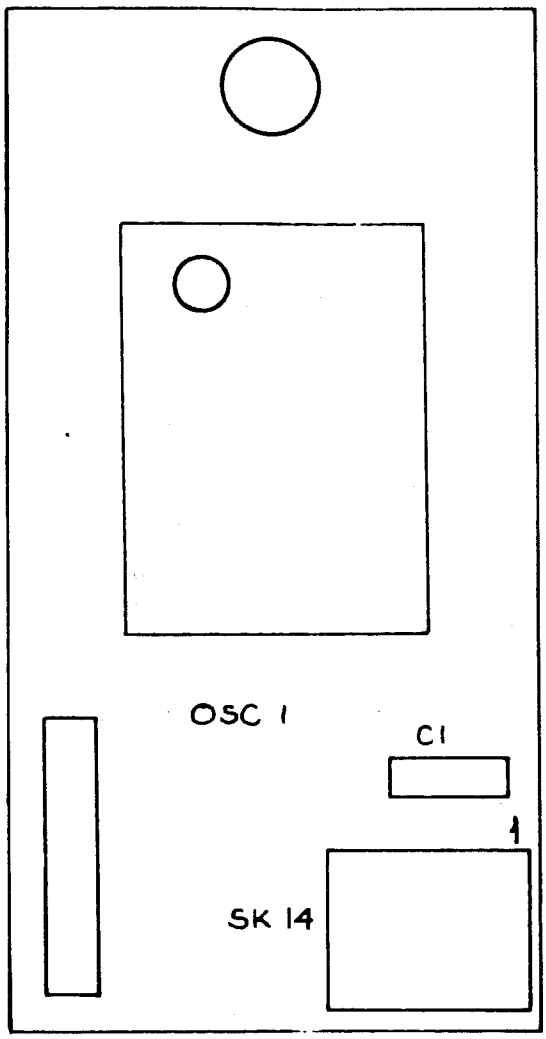
Circuit Diagram
BNC Mounting Assembly Fig. 21



Layout Diagram
BNC Mounting Assembly 19-3026 Fig. 22



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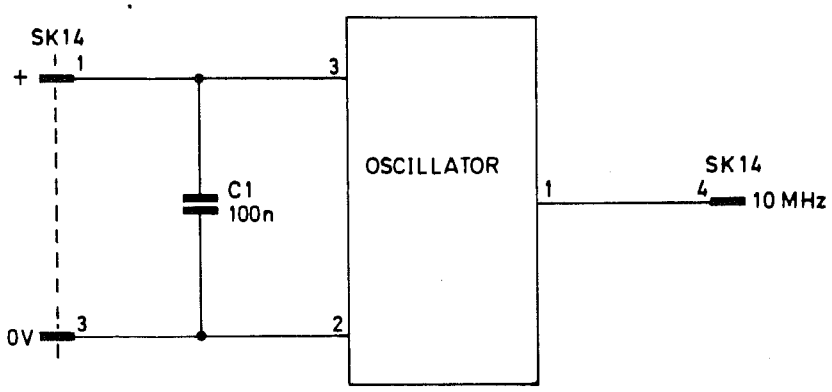
1

Component Layout:
Oscillator Assembly 19-1147

Fig. 23



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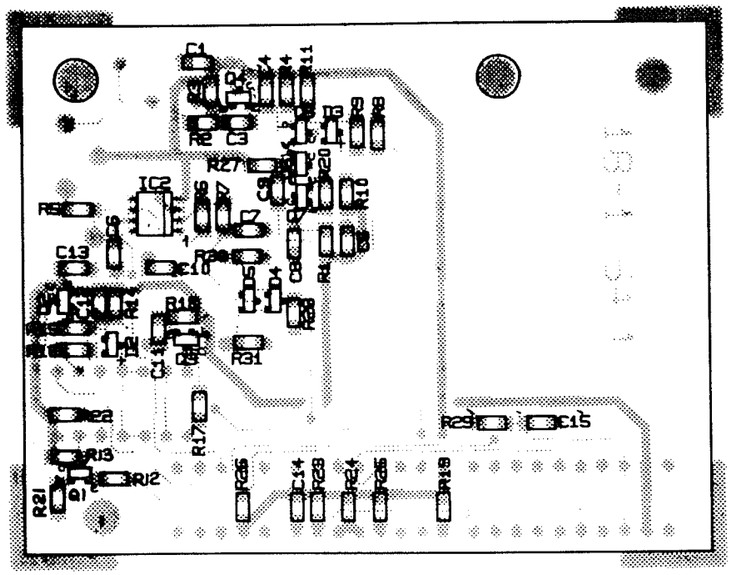
1

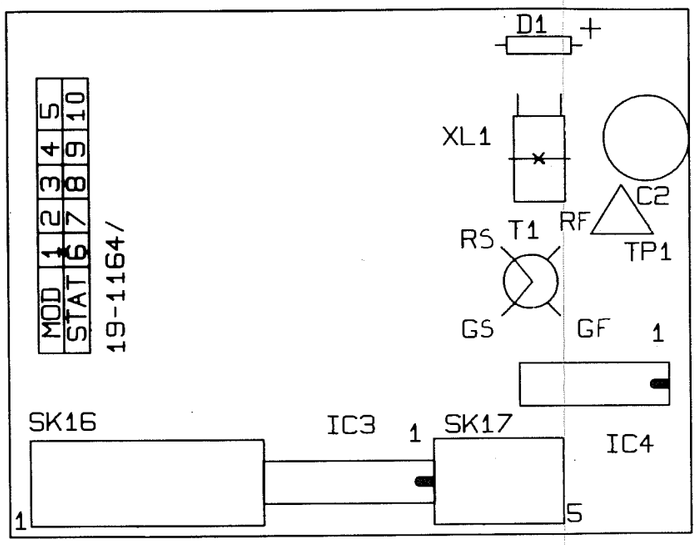
Circuit Diagram
Oscillator Assembly 19-1147

Fig. 24

TRACKSIDE VIEW



COMPONENT SIDE VIEW



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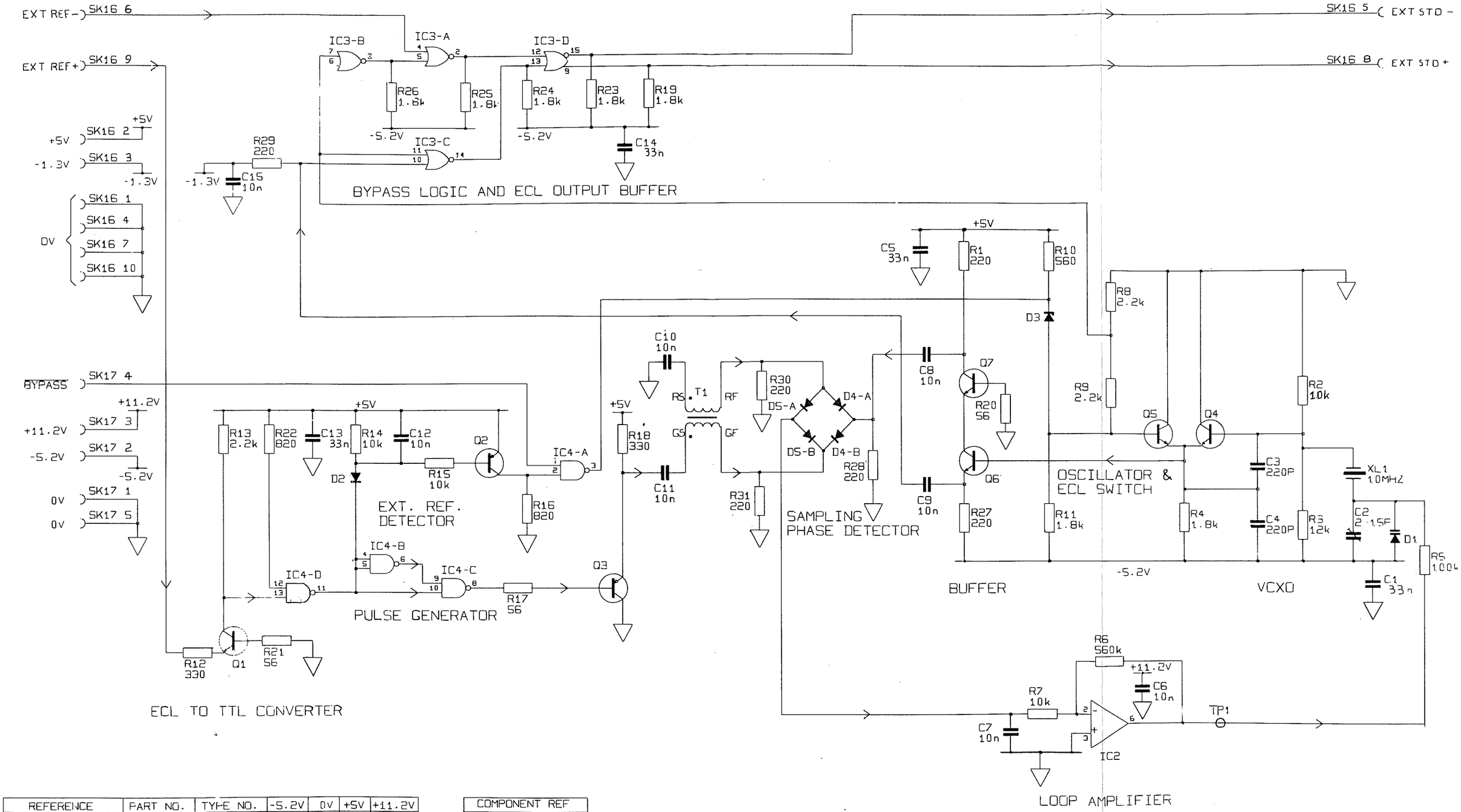
Component Layout:
Frequency Multiplier Assembly 19-1164 Fig. 25



REFERENCE	PART NO.	TYPE NO.	-5.2V	0V	+5V	+11.2V
D2	22-1093	BAS16				
D4.5	22-1096	BAV99				
D1	22-1097	MV1640				
D3	22-1882	BZX84C4V7				
IC2	22-4292	FFC2741UC	4			7
IC3	22-4514	MC10102	8	1.16		
IC4	22-4582	74LS132		7	14	
Q1, 4-7	22-6197	FMMT3904				
Q2, 3	22-6199	FMMT3906				

COMPONENT REF
R1-31
C1-15
D1-5
IC2-4
Q1-7
T1
XL1
SK16,17

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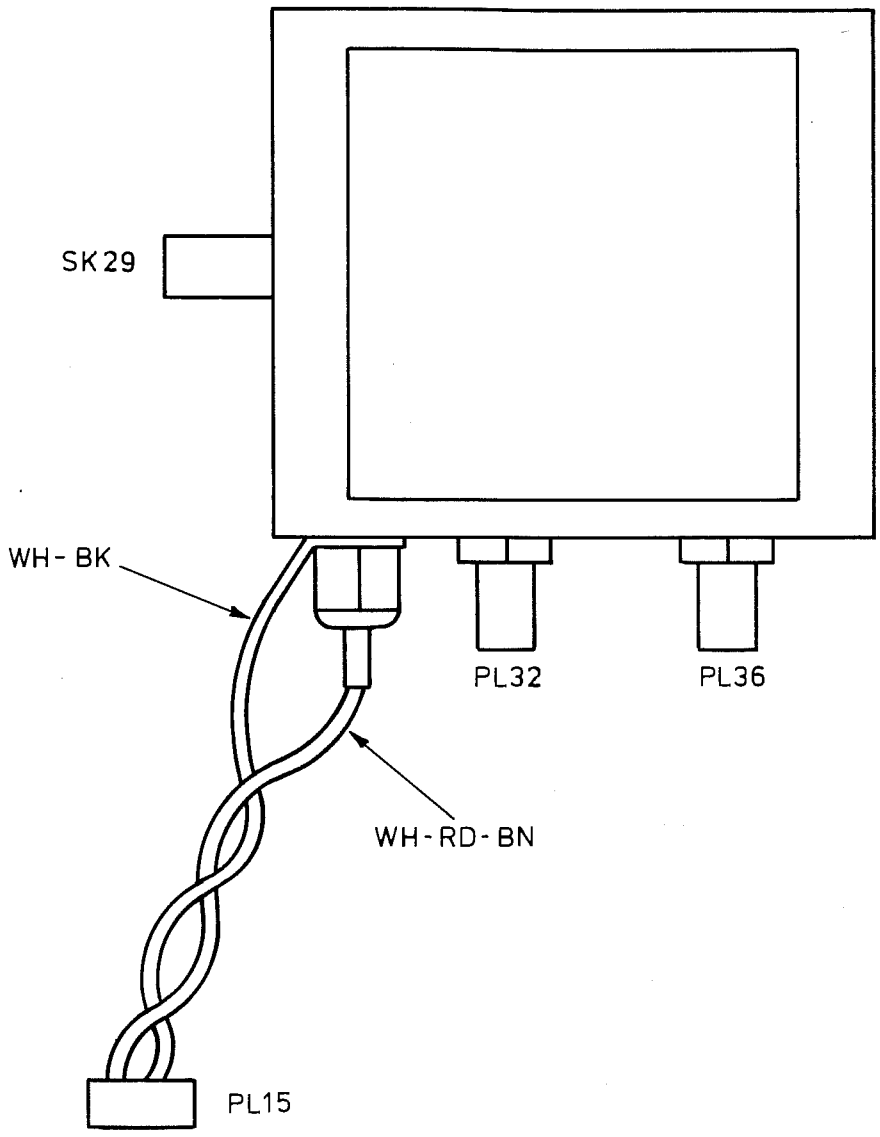
2

Circuit Diagram;
Frequency Multiplier Assembly 19-1164 Fig.26



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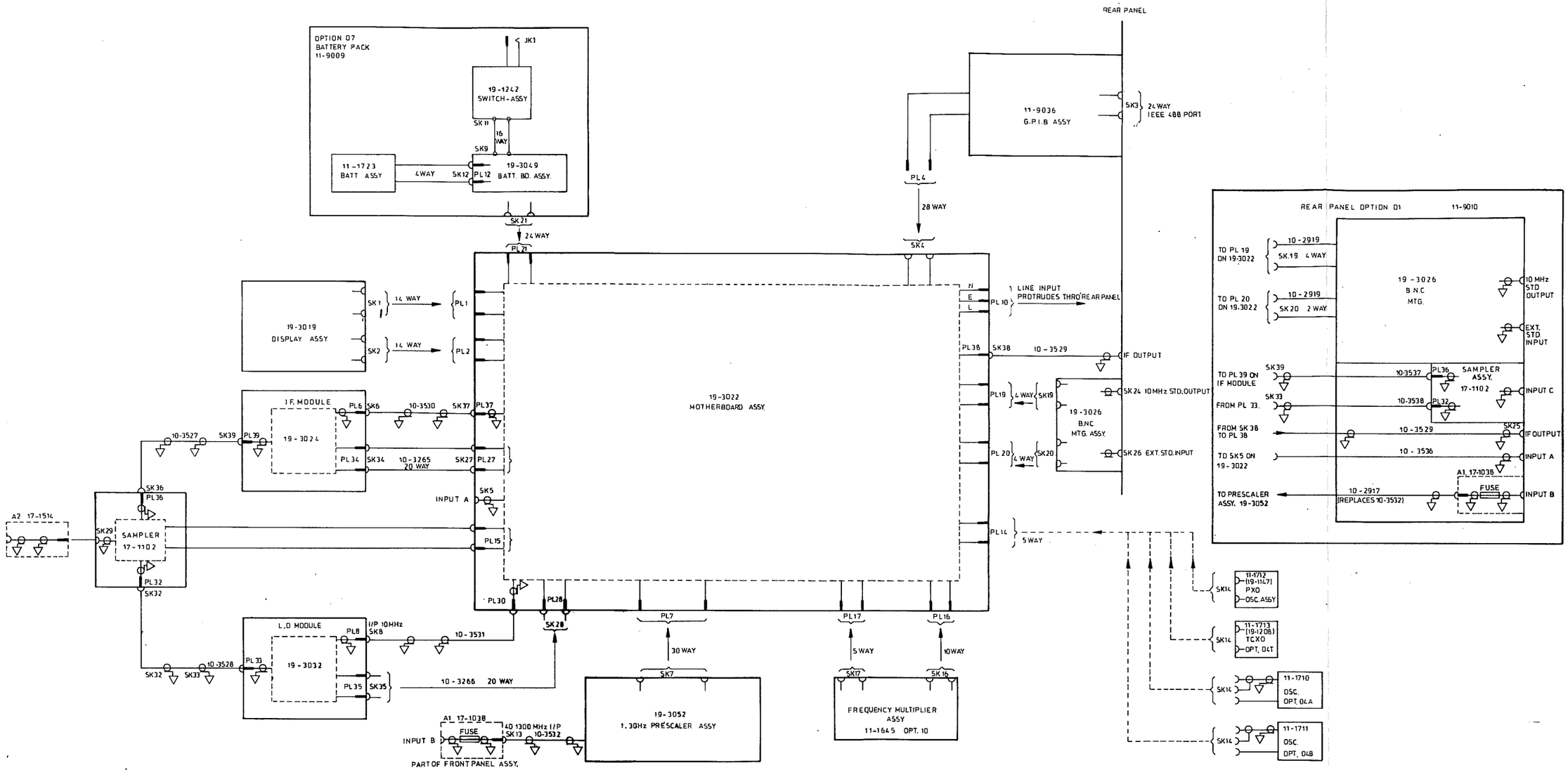
Layout :
Sampler 17-1102 Fig. 27



14 WAY	PL/SK 1
	PIN
STDBY SWITCH	14
PB4	2
PB5	6
PB6	7
PB7	5
R LED	12
A LED	1
S LED	11
STDBY LED	8
DISPLAY STROBE	4
MODE 1	3
KEY EXTEND	13

14 WAY	PL/SK 2
	PIN
-5,2V.	2
0V	7,8
+5V	10
KEYBOARD ENABLE	5
PB0	13
PB1	12
PB2	1
PB3	14
MODE 2	6
G LED GATE	11
KEY EXTEND	9
KEYBD DATA	4

24 WAY	SK3
	PIN
0V	12,18,24
NRFD	7
ATN	11
DAV	6
SRQ	10
NDAC	8
REN	17
EIO	5
IFC	9
DIO1	1
DIO2	2
DIO3	3
DIO4	4
DIO5	13
DIO6	14
DIO7	15
DIO8	16

28 WAY	SK/PL 4
	PIN
+5V	2-4
0V	25-27
RESET GPIB	28
5MHz CLOCK	24
GATE	21
GPIB OPT.	15
B0	23
B1	10
B2	12
B3	14
B4	13
B5	11
B6	9
B7	8
A0	7
A1	6
A2	5
GPIB SEL	16
GPIB DATA IRQ	22
GPIB IRQ	18
R LED	20
A LED	17
COUNTER ID	1
S LED	19

30 WAY	PL7
	PIN
+5V	23
-5,2V	6
0V (A)	4,19-22
	24-26
	28-30
GATE	17
RESET	15
U	16
B/64	8
B/32	7
B/OP	5
DET	14
B LOW	11
RST2	13
+11,2V(S)	3
+11,2V.	18
-5,2V (S)	9
B FITTED	2
KEY	1

16 WAY	SK9,11
	PIN
0V	4,5,12
NORM / BS	14
EXT. INT.	13
POWER / INT	1,2,3,
BATTERY	9,10,11

4 WAY	PL/SK 12
	PIN
BATTERY 1 0V	3
BATTERY 1 0V	1
BATTERY 2 +8V	4
BATTERY 2 0V	2

5 WAY	PL/SK 14
	PIN
+5V STDBY OSC.	1
0V	3,5
INT. REF.	4

10 WAY	PL/SK 16
	PIN
+5V STANDBY OSC	2
-9,3V	3
0V	1,4,7,10
EXT REF.-	6
EXT REF.+	9
EXT STD.+	8

5 WAY	PL/SK 17
	PIN
+15V.	3
-5,2V	2
0V	1,5
BYPASS	4

PL19 - 4 WAY SK19 - 4 WAY	PL.19	SK.19
	PIN	PIN
10 MHz STD. O/P	1	1
0V	2,3,4	2,3,4

4 WAY	PL/SK 20
	PIN
0V	1,2,3
EXT. REF. I/P	4

PL21 - 20 WAY SK21 - 20 WAY	PL 21	SK 21
	PIN	PIN
D.C. POWER	2,3,4	
SWITCHED D.C. POWER	21,23,24	
-5,2V. UR	6,19	
+5V UR.	5,20	
LINE SENSE	15	
+15V UR	18	
-11,2V UR.		
0V	9,11,13	
	14	
STDBY	16	
BATT LOW	7	
ST BY TRIG	8	
BATT SAVE TRIG	1	
KEY	17	
FAN ON	12	

20 WAY	PL/SK 27
	PIN
+15V	17,19
+5V	3,9
0V (A)	2,5,7
	10,13,15
	16
-5,2V	11,13
IF BW LCH	14
IF LVL LCH	8
IF LVL RST	6
IF BW RST	12
+5V VMF	2,4,
IF MUTE	15
POL KEY	1
IF LVL	10
IF BW	16

20 WAY	PL/SK 28
	PIN
+15V	17,19
+5VMF	1,3
0V (A)	5,7,13,15,
-5,2V	11
PB0	6
PB1	8
PB2	10
PB3	12
PB4	14
PB5	16
PB6	18
PB7	20
SYNTH LATCH EN	4
+15V(F)	19
KEY	9
LO LOCK	17
LO OFF	2
LO LATCH EN	4

	SK 7
	PIN
+5V	23
-5,2V	6
0V	4,19-22,
	24-26,28-30
1.3GHz	12
B FITTED	2
GATE	17
RESET	15
ST SL OR U	16
B LOW	11
RST 2	13
PST 1	1
DET.	14
B O/P	5
B/64	7
B/32	8

	PL 34
	PIN
+15VF	17, 19
+ 5VMF	2, 4
- 5,2V	13, 11
+ 5V	3, 9
0V	5, 7
0V (A)	18 20,
IF MUTE	15
IF BW	16
IF BW LCH	14
IF BW RST	12
IF LVL	10
IF LVL LCH	8
IF LVL RST	6
POL KEY	1

	PL 35
	PIN
LO OFF	2
+15VF	19
+5VMF	1, 3
-5,2V	11
LO LATCH EN	4,
PB0 - PB7	6,8,10,12,
	14,16,18,20
KEY	9
LO LOCK	17

PL 15	
	PIN
+12V	2
-5,2V	1
-5V	3
0V	4,5
OVLD LCH	7
OVLD RST	8
KEY	6

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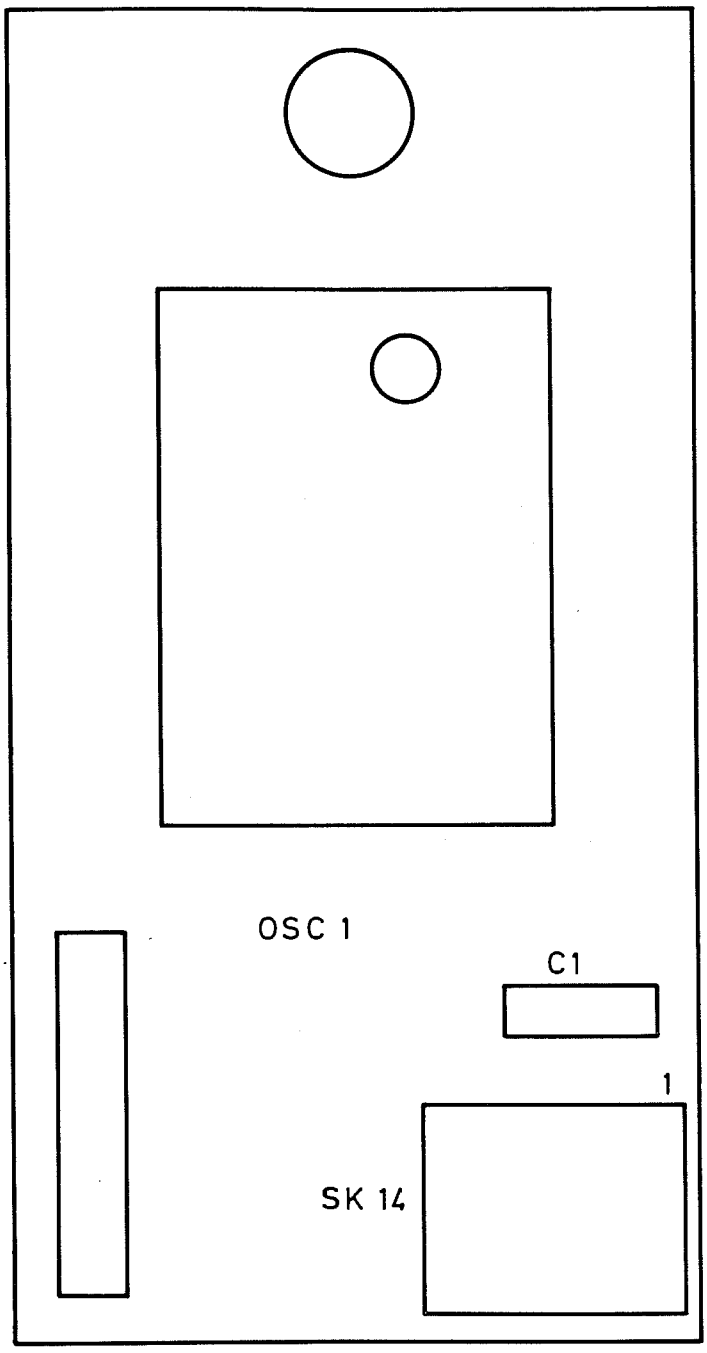
Interconnections Fig. 28



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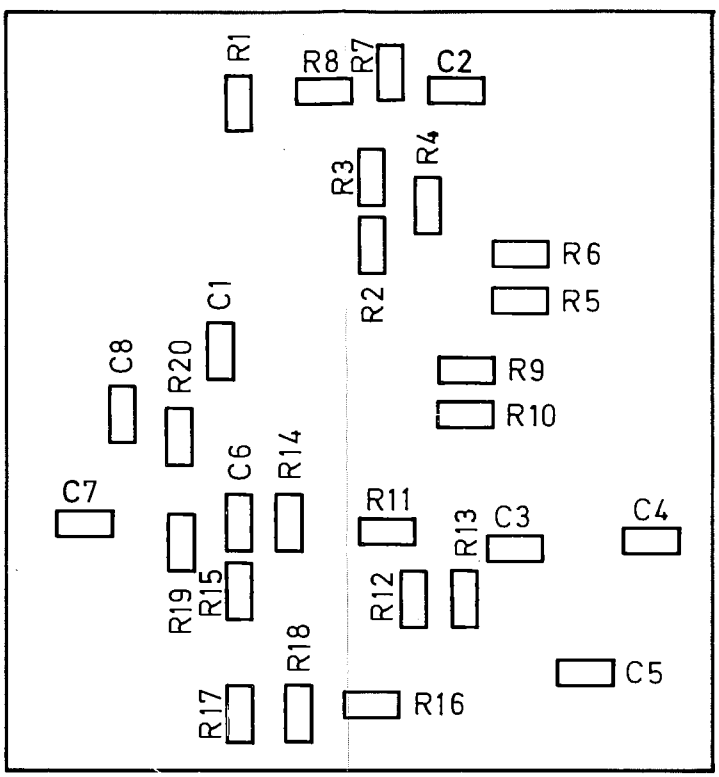
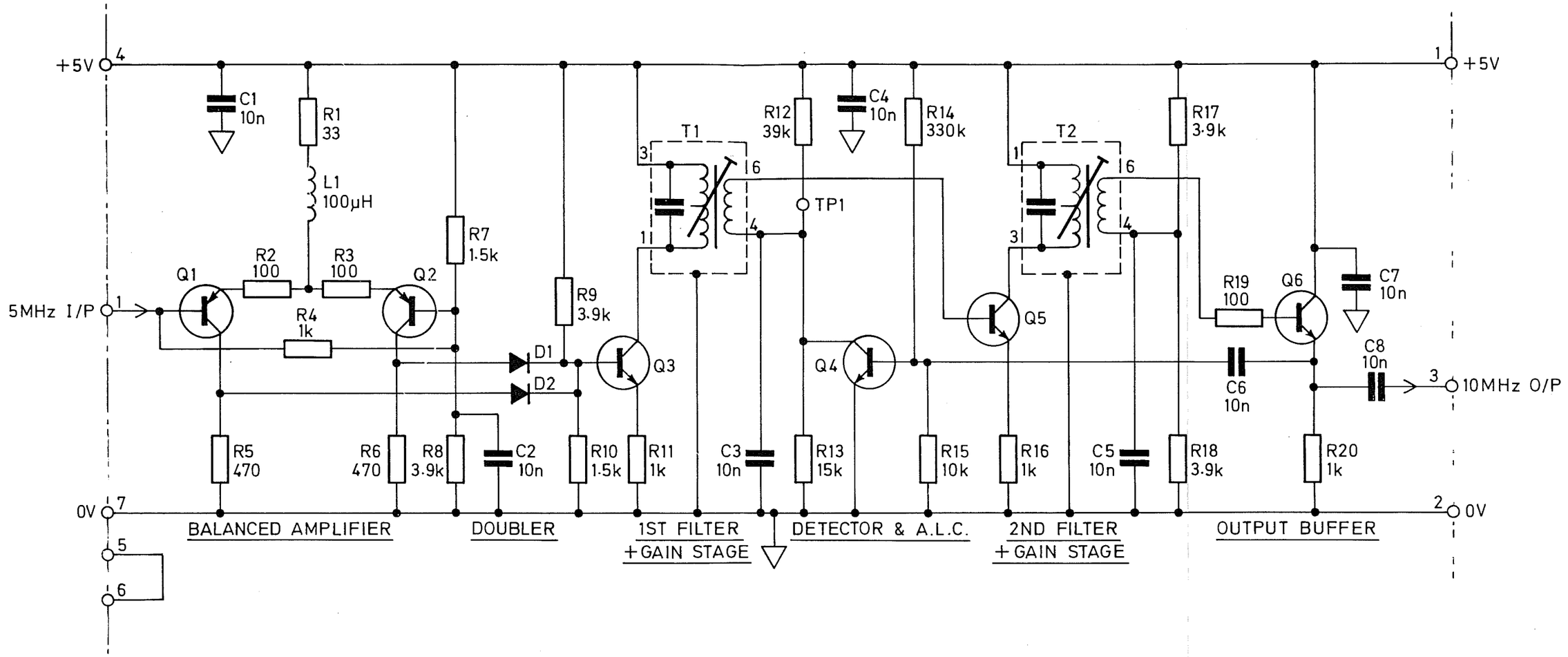
Component Layout:
Oscillator Assembly 19-1208

Fig 29



VIEWED FROM TRACK SIDE

Component Layout: Reference
Frequency Doubler Assembly 19-1238 Fig 30



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Circuit Diagram: Reference
Frequency Doubler Assembly 19-1238 Fig 31